# Exhibit D

**Chelsea Saylors - Activity in Case 2:06-cv-00151-TJW Fairchild Semiconductor Corporation et al v. Power Integrations, Inc. "Amended Complaint"**

**From:** <txedCM@txed.uscourts.gov>
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**Subject:** Activity in Case 2:06-cv-00151-TJW Fairchild Semiconductor Corporation et al v. Power Integrations, Inc. "Amended Complaint"

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**U.S. District Court [LIVE]**

**Eastern District of TEXAS LIVE**

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The following transaction was received from Smith, Michael Charles entered on 5/19/2006 at 5:09 PM CDT and filed on 5/19/2006

**Case Name:** Fairchild Semiconductor Corporation et al v. Power Integrations, Inc.
**Case Number:** 2:06-cv-151
**Filer:** Intersil Corporation
Fairchild Semiconductor Corporation
**Document Number:** 8

**Docket Text:**
AMENDED COMPLAINT against Power Integrations, Inc., filed by Fairchild Semiconductor Corporation, Intersil Corporation. (Attachments: # (1) Exhibit A# (2) Exhibit B# (3) Exhibit C# (4) Exhibit D# (5) Exhibit E# (6) Exhibit F)(Smith, Michael)

The following document(s) are associated with this transaction:

**Document description:**Main Document
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-0
] [88a1215a2b99799afb413ce4a067a90ba62b8c14fa4c8964dac651aafdafd74cbde
4fe7746686f750221d9f73a7a3bc3c41a5f5fda56e61944349eb2fe7368ca]]
**Document description:**Exhibit A
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-1
] [8c610eb0a7fc55975ac86de8c931b970d7207e37a377a3645fccb9eb631469cde19
09f889a0cde9a4d2c0d6807b2b1d9b8531c6c82456055d6466e7a4b67933c]]
**Document description:**Exhibit B
**Original filename:**n/a

**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-2
] [62b9281dc01d96b7f5edd4079e896788e22b315edeaeb8f98752eed22e625903c62
dfca09fd25182169eb3507bd87085b4d9eaaad6a876dcb1295934ff443593]]
**Document description:**Exhibit C
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-3
] [914238d8f4c272868963d1b6b03fd73bdbc29e6ff5d7181bd345151906c7b42fd31
2f04beb3b612ab745fae9ce754c6b3d470c4bd95a9235930d2d874303417d]]
**Document description:**Exhibit D
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-4
] [a6c334668c5cbfcf29a0ad7d79859d5a2ba865ebd7dade5c85e55582b75960ea63f
480f9c2b735aeea0b60d05768edad54feac165874f36cd57e965482499782]]
**Document description:**Exhibit E
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-5
] [635b4bda9b5bfbe14a0b8ce8efb58e33f152724b38fbbdf37c0a2cd9dbd29990502
3ce822d6e496e9b9897c72d05a83c41c5ce1f59e5fdc9d83f869e9dfc6976]]
**Document description:**Exhibit F
**Original filename:**n/a
**Electronic document Stamp:**
[STAMP dcecfStamp_ID=1041545818 [Date=5/19/2006] [FileNumber=1269788-6
] [3dc4de4717c0a75a96e23fbf73a771212b47477dd24738c2081f26cc1a7a9b15614
5b8b93fd399f9eadd63ac9f135852abb9ab9db1033a73fb88ef0d12a13925]]

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**2:06-cv-151 Notice will be delivered by other means to:**

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS

| | |
|---|---|
| FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation, INTERSIL AMERICAS, INC., a Delaware corporation and INTERSIL CORPORATION, a Delaware corporation<br>Plaintiff,<br>v.<br>POWER INTEGRATIONS, INC., a Delaware corporation,<br>Defendants. | **JURY**<br>**CIVIL ACTION NO. 2:06-cv-151** |

**PLAINTIFFS' AMENDED COMPLAINT**

Plaintiffs FAIRCHILD SEMICONDUCTOR CORPORATION (hereinafter, "Fairchild"), INTERSIL AMERICAS, INC. and INTERSIL CORPORATION, (Intersil Americas, Inc. and Intersil Corp. are collectively "Intersil") by and through their undersigned counsel, hereby alleges as follows:

**THE PARTIES**

1. Fairchild Semiconductor Corporation is a Delaware corporation with its principal place of business in South Portland, Maine.

2. Intersil Corporation is a Delaware corporation with its principal place of business in Milpitas, California.

3. Intersil Americas, Inc. is a Delaware corporation with its principal place of business in Milpitas, California.

4. Power Integrations, Inc. is a Delaware is a Delaware corporation with its principal place of business in San Jose, California.

## JURISDICTION AND VENUE

5. This is an action arising under the patent laws of the United States, Title 35 of the United States Code. This court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

6. Upon information and belief, this Court has personal jurisdiction over the defendant because Power Integrations sells the accused devices within this district.

7. Upon information and belief, venue is proper in the Court pursuant to 28 U.S.C. § 1391(b) and (c) and § 1400 as the defendant is subject to personal jurisdiction in this district.

## FIRST CAUSE OF ACTION

### INFRINGEMENT OF U.S. PATENT NO. 5,264,719

8. The allegations of paragraphs 1-7 are incorporated as though fully set forth herein.

9. U.S. Patent No. 5,264,719 (the "'719 Patent"), entitled *High Voltage Lateral Semiconductor Device*, duly and lawfully issued on November 23, 1993 and was assigned to Harris Corporation. A true and correct copy of the '719 Patent is attached hereto as Exhibit A.

10. Upon information and belief, on or about September 27, 1999 the '719 Patent was assigned by Harris Corporation to Intersil Corporation. A true and correct copy of that assignment is attached as Exhibit B.

11. Upon information and belief, on or about April 14, 2006, Intersil Corporation changed its name to Intersil Communications, Inc. A true and correct copy of the restated certificate of incorporation is attached as Exhibit C.

12. Upon information and belief, on or about April 14, 2006 the '719 Patent was assigned by Intersil Communications, Inc. to Intersil Americas, Inc. A true and correct copy of that assignment is attached as Exhibit D.

13. On or about March 30, 2006, Fairchild Semiconductor Corporation and Intersil Corporation entered into a Patent License Agreement that gave Fairchild the right to assert the

'719 Patent against Power Integrations. A redacted copy of that Patent License Agreement is attached as Exhibit E.

14. On or about May 17, 2006, Fairchild Semiconductor Corporation, Intersil Corporation, and Intersil Americas, Inc. entered into a Supplemental Agreement effective March 30, 2006 that gave Fairchild the right to assert the '719 Patent against Power Integrations. A true and correct copy of that Supplemental Agreement is attached as Exhibit F.

15. Upon information and belief, Power Integrations has been and is now infringing the '719 Patent, both literally and under the doctrine of equivalents, by making, using, selling, offering for sale, and importing devices and products in the United States covered by one ore more claims of the '719 Patent.

16. Upon information and belief, Power Integrations has been and is now inducing infringement and contributing to the infringement of the '719 Patent, both literally and under the doctrine of equivalents, by inducing or contributing to the making, using, selling, offering for sale, and importing by others devices and products in the United States covered by one or more claims of the '719 Patent.

17. Power Integrations' infringement has caused irreparable injury to Fairchild and Intersil and will continue to cause irreparable injury until Power Integrations is enjoined from further infringement by the Court.

**PRAYER FOR RELIEF**

WHEREFORE, FAIRCHILD and INTERSIL pray for the following relief:

A. Judgment by the Court that Power Integrations directly infringes the '719 Patent;

B. Judgment by the Court that Power Integrations induces or contributes to others' infringement of the '719 Patent;

C. Preliminary and permanent injunctive relief pursuant to 35 U.S.C. § 283 enjoining Power Integrations, its officers, agents, servants, employees, successors, assigns and all other persons or entities acting in concert or participation with Power Integrations or on Power Integrations' behalf from further infringement of the '719 Patent;

D. Money damages sustained as a result of Power Integrations' infringement of the '719 Patent;

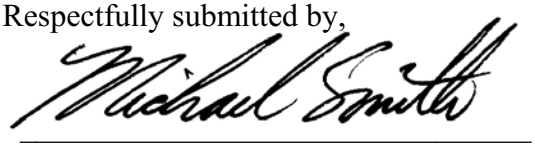
E. Costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C. § 285; and,

F. Such other relief as the Court finds just and proper.

**DEMAND FOR JURY TRIAL**

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Fairchild Semiconductor Corporation and Intersil Corporation hereby demand a trial by jury on this action.

Respectfully submitted by,



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**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 19th day of May, 2006. Any other counsel of record will be served by facsimile transmission and/or first class mail.

Michael C. Smith

US005264719A

# United States Patent [19]

Beasom

[11] Patent Number: 5,264,719

[45] Date of Patent: Nov. 23, 1993

[54] **HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE**

[75] Inventor: **James D. Beasom**, Melbourne Village, Fla.

[73] Assignee: **Harris Corporation**, Melbourne, Fla.

[21] Appl. No.: **705,509**

[22] Filed: **May 24, 1991**

**Related U.S. Application Data**

[63] Continuation of Ser. No. 242,405, Sep. 8, 1988, abandoned, which is a continuation-in-part of Ser. No. 831,384, Jan. 7, 1986, Pat. No. 4,823,173.

[51] **Int. Cl.**[5] ..... **H01L 29/80**

[52] **U.S. Cl.** ..... **257/335**; 257/336; 257/339

[58] **Field of Search** ..... 357/38, 55, 23.8, 46

[56] **References Cited**

U.S. PATENT DOCUMENTS

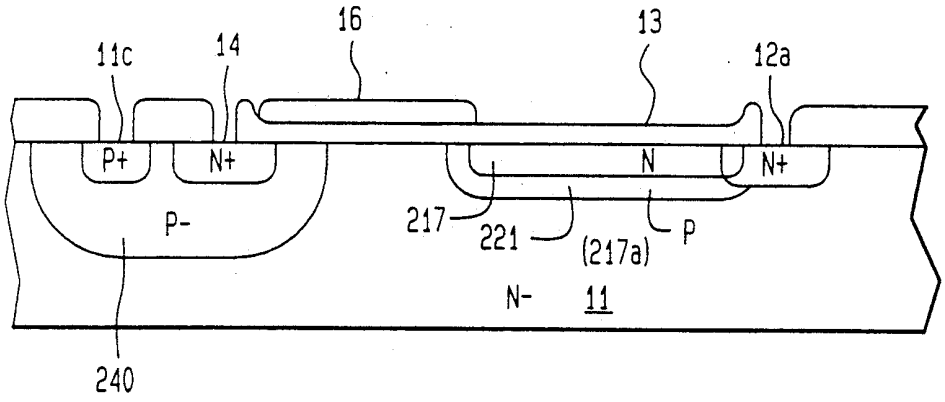
| | | | |
|---|---|---|---|
| 4,626,879 | 12/1986 | Colak | 357/23.8 |
| 4,628,341 | 12/1986 | Thomas | 357/23.8 |
| 4,811,075 | 3/1989 | Eklund et al. | 357/46 |
| 4,994,889 | 2/1991 | Takeuchi et al. | 357/55 |
| 4,994,904 | 2/1991 | Nakagawa et al. | 357/38 |

*Primary Examiner*—Rolf Hille
*Assistant Examiner*—Roy Potter
*Attorney, Agent, or Firm*—Evenson, Wands, Edwards, Lenahan & McKeown

[57] **ABSTRACT**

The present invention provides an improved lateral drift region for both bipolar and MOS devices where improved breakdown voltage and low ON resistance are desired. A top gate of the same conductivity type as the device region with which it is associated is provided along the surface of the substrate and overlying the lateral drift region. In an MOS device, the extremity of the lateral drift region curves up to the substrate surface beyond the extremity of the top gate to thereby provide contact between the JFET channel and the MOS channel.

**42 Claims, 7 Drawing Sheets**



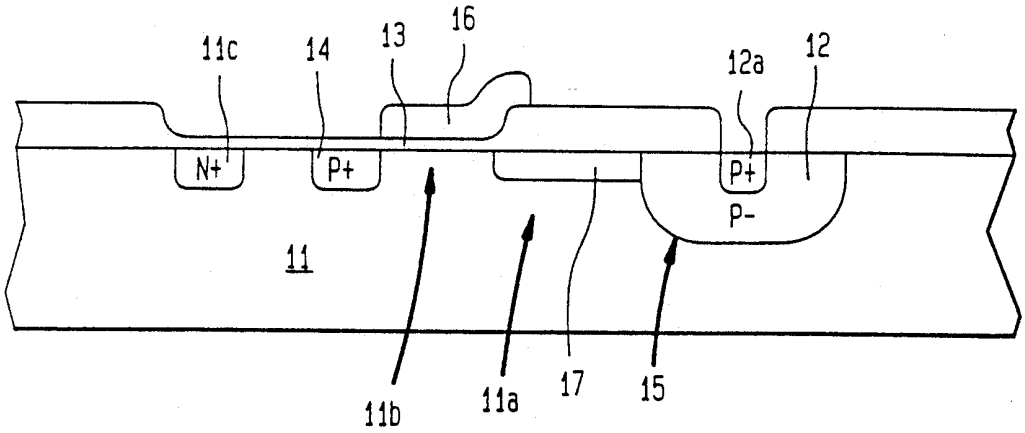



FIG. 1

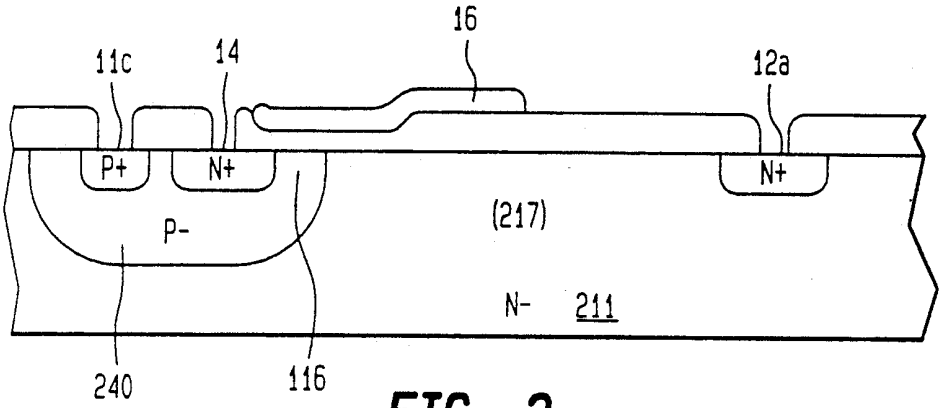



FIG. 2
(PRIOR ART)

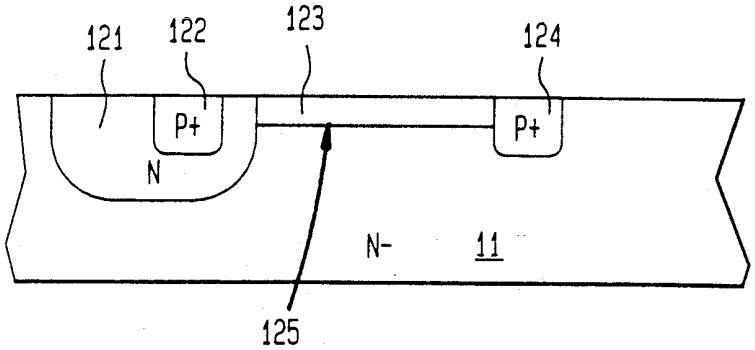



FIG. 3

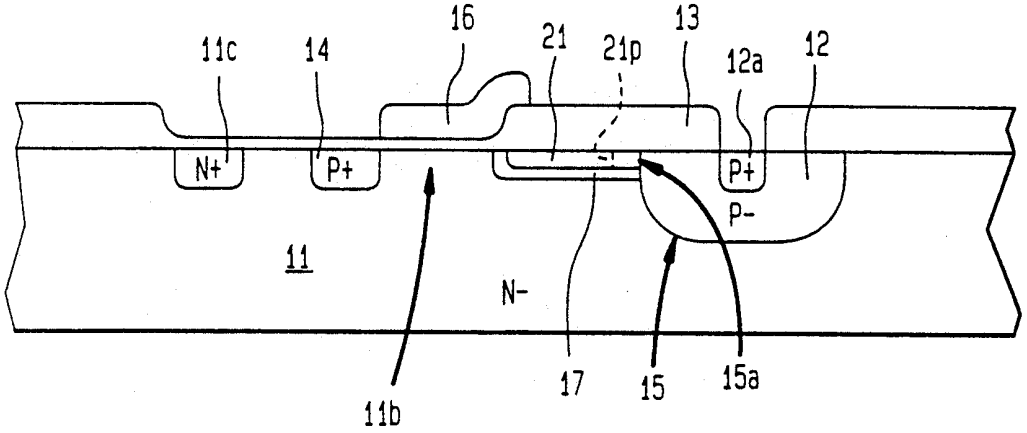

16
11c
14
21
21p
13
12a
12
N+
P+
P+
P-
11
N-
11b
17
15
15a

FIG. 4

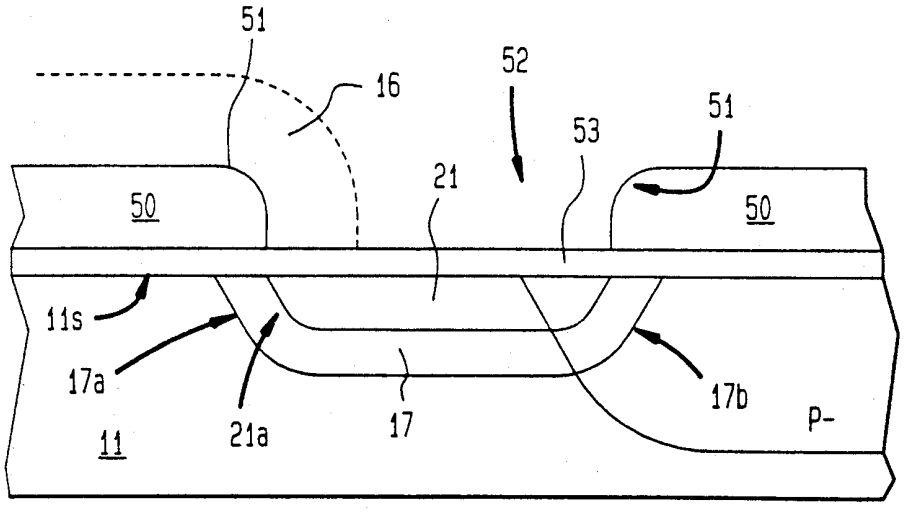

51
16
52
53
51
21
50
50
11s
17a
21a
17
17b
P-
11

FIG. 5

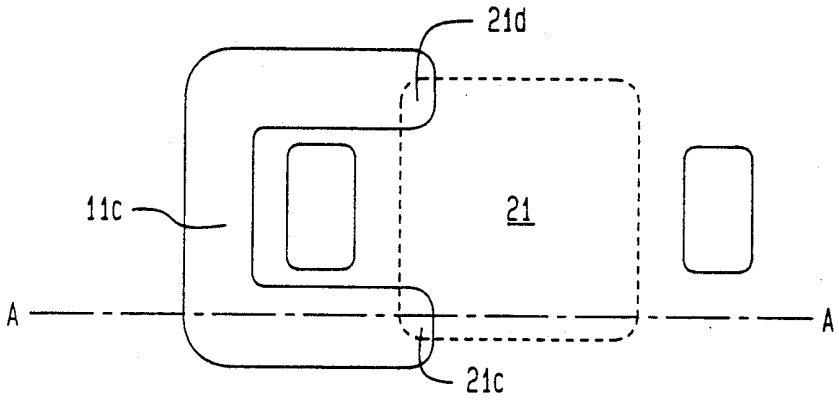



FIG. 6a

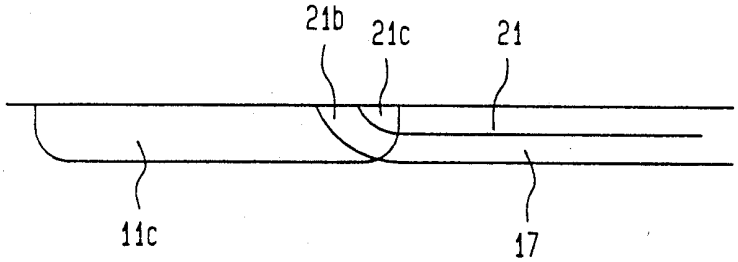



FIG. 6b

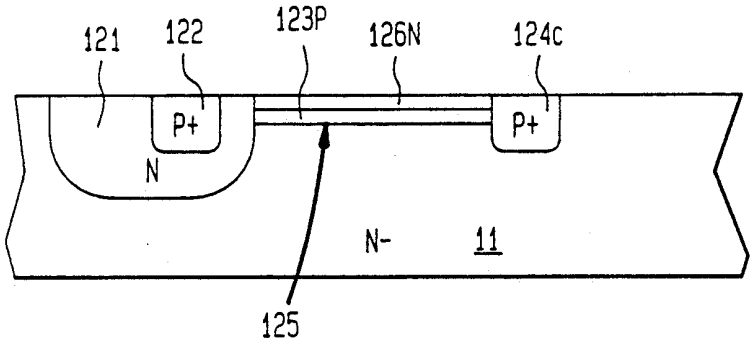

121
122
123P
126N
124c
P+
P+
N
N-
11
125

FIG. 7

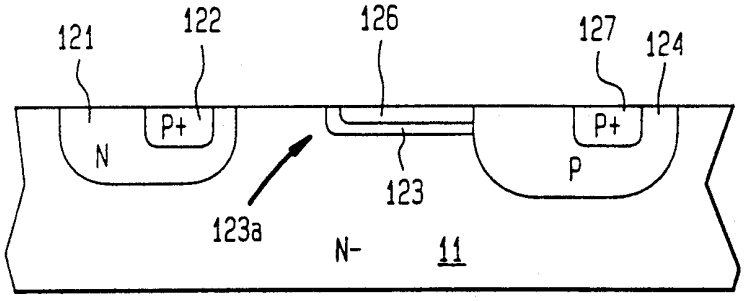

121
122
126
127
124
P+
P+
N
P
123
123a
N-
11

FIG. 8

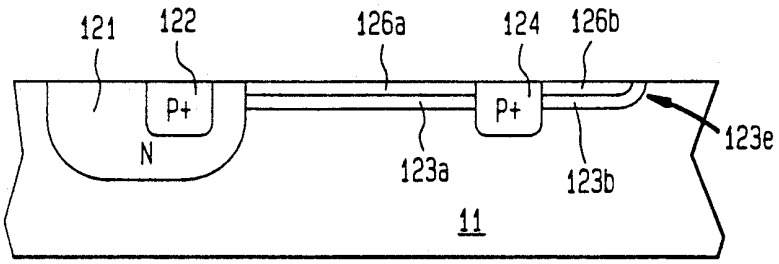

121
122
126a
124
126b
P+
P+
N
123a
123b
123e
11

FIG. 9

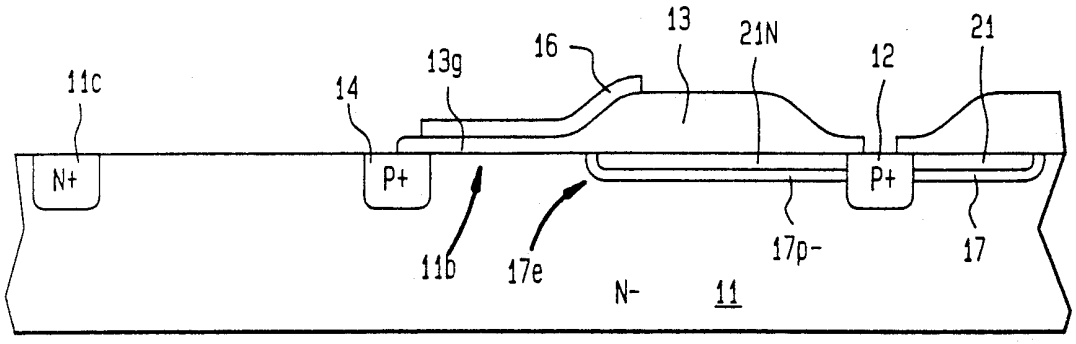

11c
14
13g
16
13
21N
12
21
N+
P+
P+
11b
17e
17p-
17
N-
11

FIG. 10

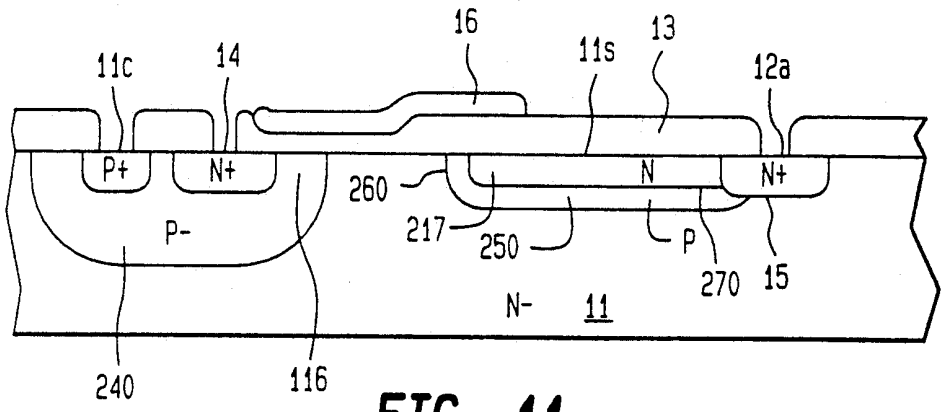

16
11c
14
11s
13
12a
P+
N+
260
N
N+
P-
217
250
P
270
15
N- 11
240
116

FIG. 11

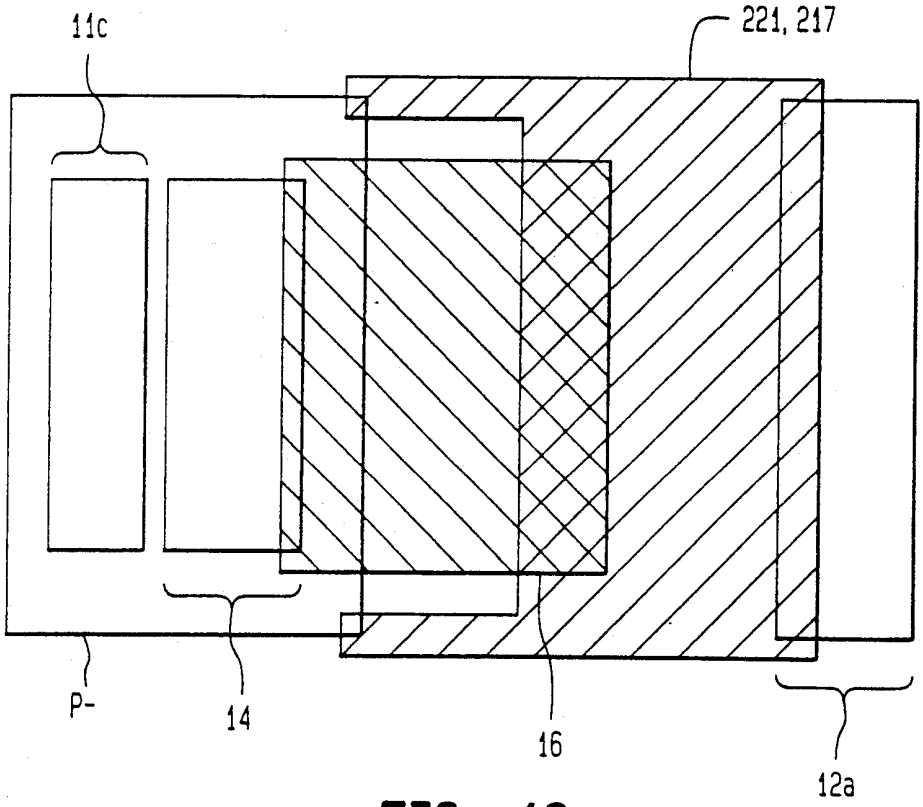

11c
221, 217
P-
14
16
12a

FIG. 12

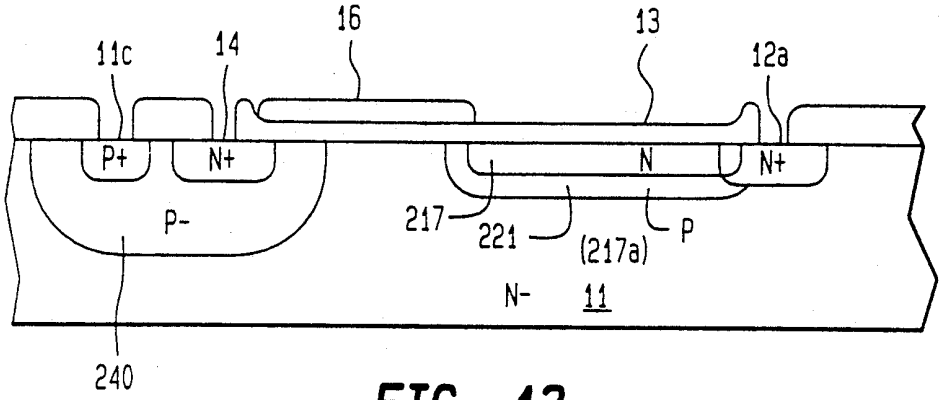

16
13
11c
14
12a
P+
N+
N
N+
P-
217
221
(217a)
P
N- 11
240

FIG. 13

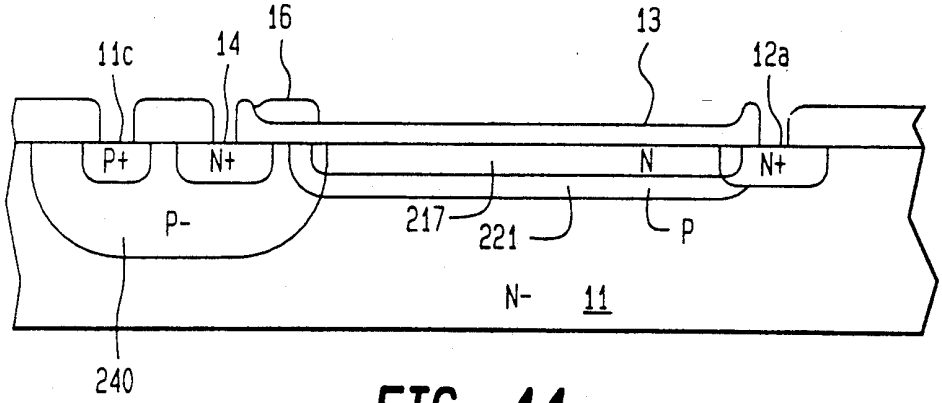

16
13
11c
14
12a
P+
N+
N
N+
P-
217
221
P
N- 11
240

FIG. 14

# HIGH VOLTAGE LATERAL SEMICONDUCTOR DEVICE

This is a continuation of application, Ser. No. 242,405, filed Sep. 8, 1988, now abandoned which, in turn, is a continuation-in-part of application, Ser. No. 831,384, filed Jan. 7, 1986, now U.S. Pat. No. 4,823,173, issued Apr. 18, 1989.

## FIELD OF THE INVENTION

The present invention relates to lateral semiconductor devices and an improved method of making lateral semiconductor devices. More specifically, the invention relates to high voltage lateral devices with reduced ON resistance and a method of making such devices.

Previous high voltage lateral devices include both MOS devices and bipolar transistors. For example, FIG. **1** illustrates a known structure which can be used as a high voltage lateral MOS device. This device is known as a lateral drift region MOS device and is dependent upon the drain-to-body junction **15** as the basic high voltage junction of the device. The drift region **17** is a P region along the top surface of the N− substrate **11** and is located so as to lie adjacent the P− drain region **12**. The drift region **17** is used to connect the high voltage drain **12** to the gate **16** and source **14**. The two contacts, drain contact $12_a$ and body contact $11_c$ are shown for completeness. In the operation of this circuit, the gate **16** and source **14** never assume large voltages relative to the body **11**. The drift region **17** serves as a JFET channel with the portion $11_a$ of body region **11** underlying the channel acting as a JFET gate. The JFET channel **17** is designed to totally deplete when the drain **12** is reverse biased to a voltage less than the voltage necessary to reach critical field in the channel-to-body depletion layer. This design preserves the effective high breakdown voltage of drain body junction **15**. Also the source **14** and gate **16** (over the gate oxide **13**) are safely shielded from the high drain body voltage by the pinched off JFET channel **17**.

The resistance of the lateral drift region JFET channel **17** is in series with the resistance of the MOS channel $11_b$, consequently the total channel resistance of the device is the sum of these two individual resistances. The JFET channel, which must be quite long to sustain high drain body voltages, is often the larger of the two resistance terms. Thus it is desirable to find ways to reduce the resistance of the drift region so that devices of a given size can be made with smaller channel resistance.

FIG. **2** illustrates a known structure which can be used as a high voltage lateral DMOS (LDMOS) device. In this device, an N+ drain contact **12A** is formed in the N− substrate **211** and an N+ source **14** and P+ body contact $11_c$ are formed in a P− body region **240**. The drift region **217** is an N− region along the top surface of the N− substrate **211** which connects the drain **12** to the gate **16** and source **14**. In this high voltage device, the N− drift region **217** must be lightly doped to obtain high body **240** to drain breakdown.

The ON resistance of the LDMOS is approximately the sum of the channel resistance and the bulk resistance in the N− drift region **217**. The lateral distance from the N+ drain **12** to the adjacent edge of the MOS channel $11_b$ underlying the gate on the P− body **240** must be large to allow space for the reverse bias depletion layer which spreads from the body-to-drain junction into the lightly doped drain. This distance, along with the high N− resistivity contribute to the high drift region resistance, which is often much greater than the channel resistance. Thus, it is desirable to reduce the drift region resistance of the LDMOS device.



FIG. **3** shows a known structure which can be used as a lateral bipolar transistor. Another illustration of such a device is contained in FIG. 7 of U.S. Pat. No. 4,283,236 issued Aug. 11, 1981. Referring to FIG. **3**, an N− substrate **11**, has an N type emitter shield **121** formed therein and P+ emitter **122** and collector **124** formed as shown. Additionally, a P− drift region **123** is provided along the surface of the substrate between the collector **124** and the emitter shield **121**. In the operation of this device, the total collector resistance is equal to the sum of the resistance across the drift region **125** plus the resistance of the P+ collector between the drift region and the collector contact. In order to provide devices of equal size having a lower collector resistance, it is desirable to find ways to reduce the resistance of the drift region.

In the operation of this device, the drift region extends the collector to the edge of the emitter shield, **121**, so that the base width is just that small distance between the adjacent edges of the emitter, **121**, and the drift region, therefore, providing improved frequency response.

At high base-collector voltages, the drift region, **123**, depletes by JFET action with the N-base, **11**, and N shield, **121**, which is part of the base, acting as gate before critical field is reached just as for the MOS of FIG. **1**. This preserves the high breakdown of the structure.

## SUMMARY OF THE INVENTION

The present invention provides a structure having a reduced channel resistance and a process capable of efficiently obtaining the structure of the invention. The reduction in channel resistance is accomplished by providing a top gate which is located between the lateral drift region of the prior art and the surface of the channel region and which may be in contact with the high voltage device region. This top gate allows the total channel doping to be increased because the top gate to channel depletion layer holds some additional channel charge when reverse biased in addition to that held by the bottom gate to channel depletion layer of the prior art structure. The ionized channel impurity atoms associated with this additional channel charge causes the reduction in channel resistance.

With respect to providing an improved LDMOS structure having a lower drift region resistance, a second drift region which is separated from the original drift region by a region of opposing conductivity is formed. The second drift region provides a conductive path which is in parallel with the original drift region thereby achieving the desired reduction in resistance. Because of the formation of the second drift region, the first enclosed drift region can now have a much higher doping than the second drift region which it replaces, while achieving the same breakdown voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross section of a known MOS device having typical ON resistance.

FIG. **2** is a cross section of a known LDMOS device having typical ON resistance.

FIG. 3 is a cross section of a known bipolar transistor having typical collector resistance.

FIG. 4 is a cross section of an MOS device including the improved drift region and top gate of the invention.

FIG. 5 illustrates optimized process steps for obtaining the desired shape of the top gate and drift region of the invention.

FIGS. 6*a* and 6*b* are, respectively, a top view and a cutaway perspective view of the body contact extending through the top gate and drift region of the invention.

FIG. 7 is a cross section of a bipolar device made in accordance with one aspect of the invention.

FIG. 8 is a cross section of a bipolar device made in accordance with another aspect of the invention.

FIG. 9 is a cross section of a bipolar device made in accordance with a preferred aspect of the invention.

FIG. 10 is a cross section of an MOS device, including the lateral drift region and top gate of the invention, in a preferred embodiment.

FIG. 11 is a cross section of a LDMOS device made in accordance with a preferred embodiment of the invention.

FIG. 12 is a top view of the LDMOS device of FIG. 11.

FIG. 13 is a cross section of a LDMOS device made in accordance with another preferred embodiment of the invention.

FIG. 14 is a cross section of a LDMOS device made in accordance with still another preferred embodiment of the invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention is described herein with reference to the drawings for both MOS and bipolar applications. FIG. 4 shows an MOS device where $P^+$ drain contact $12_a$ is formed in $P^-$ type drain **12**, $P^+$ source **14** is formed in the $N^-$ body **11** and $N^+$ body contact $11_c$ is provided in the $N^+$ body **11**. The MOS channel region $11_b$ is in the $N^-$ body **11** below the MOS gate **16**. The N type top gate **21** is provided along the surface $11_s$ of the body **11** above the P type drift region **17** which acts as a JFET channel. The lateral edge or peripheral edge of both the top gate **21** and drift region **17** extend to the drain-to-body junction **15** and preferably terminate at the junction **15**. It is noted that situations may exist where the doping level in the top gate may be sufficiently high so as to render it desirable to provide a shorter top gate having a lateral extension which stops short of contacting the junction **15**. In this case care should be taken to insure that any nondepleted portion of the top gate does not result in a breakdown of the top gate-to-drift region junction 17A. Proper doping of the top gate **21** will generally be a sufficient preventative step. Dashed line $21_p$ designates the peripheral edge of top gate **21** in an embodiment where the top gate does not extend all the way to the junction **15**.

The structure of FIG. 4 provides reduced ON resistance in the JFET channel **17** relative to the prior art lateral drift MOS device as shown in FIG. 1. The reduction in ON resistance is accomplished by providing a structure which can accommodate increased drift region doping without suffering from reduced body-to-drain breakdown. This is possible because of the provision of the top gate **21**. The top gate-to-channel depletion layer which holds some channel charge when reverse biased, is in addition to the channel charge held by the bottom gate to channel depletion layer of the prior art. This additional channel charge, in the form of ionized channel impurity atoms, causes the reduction in channel resistance. It is possible to provide more than twice the doping level previously acceptable due to the additional ability to hold channel change. Thus, for a drift region **17** having a doping of $1\times10^{12}$ boron atoms per square centimeter in a bottom gate arrangement, the present invention will permit $2\times10^{12}$ boron atoms per square centimeter. Thus, the ON resistance will be only half the ON resistance of the prior arrangement.

In order to optimize performance of the structure of the invention, the top gate **21** must be designed differently than an ordinary JFET gate. Top gate **21** should become totally depleted at a body-to-drain voltage of less than the breakdown voltage of the top gate-to-drain junction **15**. Since top gate **21** is connected to body **11** (as shown in FIGS. 6A, 6B to be described below), the voltage at the top gate-to-drain junction $15_a$ will equal the voltage of the body-to-drain junction **15** voltage and the top gate-to-drain breakdown voltage should be greater than the voltage at which top gate **21** becomes totally depleted. Additionally, the top gate **21** must totally deplete before the body **11** to channel **17** depletion layer reaches the top gate **21** to channel **17** depletion layer to thereby assure that a large top gate **21** to drain **12** voltage is not developed by punch-through action from the body **11**. An ordinary JFET gate never totally depletes regardless of operating conditions.

In addition to the above described characteristics of the device of the invention, it is also necessary to insure that the channel of the JFET drift region **17** contacts the inversion layer MOS surface channel. This can be accomplished as shown in FIG. 5 where an implant mask **50** having a tapered edge **51** is provided over the body **11**. An implant aperture **52** is provided in mask **50** at the location where the P drift region **17** and N top gate **21** are to be formed. The aperture **52** is shown as exposing the protective oxide **53**. Ion implantation is not substantially affected by the oxide **53** due to the oxide thickness of only about 0.1–0.2 micrometers, yet the oxide provides surface passivation for the underlying body **11**.

The drift region **17** is ion implanted and, because of the graduated thickness of the implant mask **50** (along the edge **51**), the depth of the implanted drift region **17** is graduated or tapered. In the illustration, a fairly good rounding of the drift region **17** occurs at the peripheral edges or extremeties $17_a$, $17_b$ of the region **17**. The curved extremity $17_a$ is of interest because at this location the channel of the JFET drift region **17** contacts the surface $11_s$ of body **11** beyond the end $21_a$ of top gate **21** and is desirably beneath the gate **16** of the MOS device. The top gate **21** may be ion-implanted using the implant mask **50** but at an energy level which results in a shallower implantation. This tapered profile, particularly if curved, provides improved performance.

In a variation of this method, a diffusion process can be used to bring the JFET channel into contact with the surface of body **11**, and hence insure that the JFET channel **17** will contact the inversion layer MOS surface channel (lateral drift region **17** and top gate **21** are diffused after initial introduction by ion implant). The doping levels and diffusion times are chosen such that the extremity $17_a$ of JFET channel **17** diffuses beyond the end $21_a$ of the top gate **21** and so that the end $17_a$ reaches the surface $11_s$ of body **11**. In practice, this approach can be facilitated by choosing a top gate dop-

ant which has a lower diffusion coefficient than that of the drift region dopant.

The formation of the drift region **17** and top gate **21** may be conveniently carried out by forming a mask over the gate oxide which is present in a lateral MOS application. The MOS gate may be utilized as one delineating edge of the implant for the drift region and top gate and a thick oxide portion surrounding a thinner oxide portion may form the remainder of the implant mask. The thinner oxide portion shall be located such that it extends from beneath the MOS gate to the drain and preferably overlaps the drain. The implant mask **50** illustrated in FIG. **5** is shown as having thin oxide portion **53** being surrounded by the implant mask **50**. If the MOS gate **16** shown in dashed lines were used as a portion of the mask **50**, the edge of the drift region and top gate would be self-aligned with the MOS gate as shown in dashed lines. Then, when diffused, the drift region will extend laterally to a point beneath the MOS gate, while the top gate **21** may be formed such that there is little or no lateral overlap with the MOS gate. The extent of lateral diffusion of the top gate is dependent upon the dopant material and processing temperatures following top gate implant. It is noted that there is a separation between the drift region and the source. This separation zone is the location where the MOS channel is located.

The top gate **21** will perform as previously described if it is tied to the body **11**. Thus, the top gate **21** and the body which operates as the bottom gate of the JFET channel will be at equal potential. According to the invention, this may be accomplished in a particularly effective manner if the drift region **17** is widened to overlap with the body contact region $11_c$. This is shown in FIG. **6***a* which shows the overlapping of the top gate **21** and the body contact $11_c$ at the overlap regions $21_c$, $21_d$. In order for this arrangement to be effective, it is necessary that the body contact $11_c$ have a higher dopant concentration than the JFET channel (or drift region) **17**, as shown in FIG. **6***b* to insure that the body contact $11_c$ forms a continuous region horizontally and/or vertically through the JFET channel and to the body region **11** from the top gate, **21**.

FIG. **6***b* shows a cross section of the structure of FIG. **6***a* taken along dashed line A—A. The body **11** is provided with body contact $11_c$ which is located such that the top gate **21** and drift region **17** can be conveniently extended to overlap the body contact $11_c$. The depth of body contact $11_c$ may be made greater than the depth of region **17** such that a portion of the body contact $11_c$ extends below region **17** and provides contact with the body **11**. This arrangement provides a contact portion $21_c$ where the top gate **21** is in contact with body contact $11_c$. Thus, as long as the body contact doping concentration in region $21_b$ is sufficiently high to overcome the opposite doping in region **17**, then a good connection of uniform conductivity type will be provided between the top gate **21** and the body **11**, via contact region $11_c$. It is also noted that the body contact $11_c$ extends laterally beyond the end of both of the top gate **21** and the drift region **17**. The lateral extension of the contact $11_c$ will also provide a structure which results in a good connection of uniform conductivity type from the top gate **21** to the body **11**, again, provided that the doping of body contact $11_c$ converts region $21_b$.

Another area where the present invention finds application is in lateral bipolar transistors which employ a lateral drift region. The known structure of FIG. **3** may be improved by providing an N type top gate **126** as shown in FIG. **7**. In this arrangement the N type gate **126** extends from the collector **124** to the emitter shield **121** along the surface of body **11**. The operation of this device is enhanced by the same phenomenon as the lateral drift region of the previously described MOS device. As the base **11** becomes positive relative to the collector **124**, the top gate-to-drift region depletion layer facilitates pinch-off of the drift region **123**. However, as the base **11** becomes more negative, the top gate **126** contributes additional surface exposure to the drift region **123** and further enhances carrier transportation.

FIG. **8** shows an improvement over the arrangement shown in FIG. **7**. In FIG. **8** the drift region **123** does not extend all the way over to the emitter shield **121**. The curved end $123_a$ of the drift region **123** contacts the top surface of body **11**. It is noted that in this arrangement, the emitter shield **121** may be omitted.

An additional improvement shown in FIG. **8** is the use of a deep diffusion to form the collector **124** resulting in a significantly increased breakdown voltage. The deep diffusion step may be the same step used for forming the emitter, in which case the collector **124** shown in FIG. **7** would be deeper, or a separate collector implant and diffusion step may be employed and the collector contact **127** may then be formed simultaneously with the formation of the emitter **122**. This improvement in junction breakdown voltage is equally obtainable, for example, at the body to drain junction in the MOS devices described previously.

A further extension of the invention which may be used to increase base-to-collector breakdown voltage for a PNP device is shown in FIG. **9**. In addition to the provision of the N type top gate $126_a$ over the P− drift region $123_a$, the top gate **126A** and drift region **123A** are enlarged to surround the collector **124** and a curved edge $123_e$ is provided at the periphery of the enlarged portion $123_b$ of the drift region **123A**. This enlarged portion is designated by reference numerals $123_b$ for the drift region and $126_b$ for the top gate. The collector **124** to base **11** breakdown voltage is increased relative to alternative arrangements because of mitigation of the breakdown reduction due to the junction curvature. The top gate $126_a$ extends to the emitter shield **121** as does the drift region $123_a$. The P+ emitter **122** is formed in the N+ type emitter shield **121**.

FIG. **10** illustrates an extension of the invention with respect to a P channel MOS device similar to the improvement described with respect to the bipolar device shown in FIG. **9**. For the MOS device, the drain **12** is surrounded by the P− drift region **17** and N type top gate **21**. Around the entire periphery of the drift region **17** there is a curved portion $17_e$ which rounds up to the surface of the N− substrate **11** to insure that the JFET channel in the drift region **17** contacts the MOS channel $11_b$ under the MOS gate **16**. The drift region **17** extends outward from the entire perimeter of the drain **12**. This arrangement mitigates the breakdown reduction due to junction curvature. The P+ source **14** and N+ body contact $11_c$ are shown as is the dielectric **13** which serves as the gate oxide $13_g$ beneath the MOS gate **16**.

In both the arrangements shown in FIG. **9** and FIG. **10**, the planar diode breakdown improvement created by the drift region acting as a surface layer of the same conductivity type as the collector in FIG. **9** and drain in FIG. **10** and extending out from the perimeter of the collector and drain can be implemented by a single series of process steps. According to the invention, a

common set of process steps produces both a suitable breakdown improvement layer and an improved drift region. The breakdown improvement layer is a two layer component.

A further extension of the invention is illustrated in FIG. **11** which shows an LDMOS device where $N^+$ drain contact $12_a$ is formed in an $N^-$ type substrate and an $N^+$ source **14** and $P^+$ body contact $11_c$ are formed in a $P^-$ type body region **240**. The DMOS channel region $11_b$ is in the $P^-$ body **240** below the DMOS gate **16**. The N type first drift region **217** is provided along the surface $11_s$ of the substrate **11** above a $P^-$ type separation region **250**. A second drift region $217_a$ exists in the substrate **11** underneath the $P^-$ type separation region. The lateral edge of both the first drift region **217** and the separation region **250** extend from the gate **16** to the $N^+$ drain contact $12_a$.

The structure in FIG. **11** provides reduced ON resistance by way of the second (surface) drift region $217_a$ relative to the (deeper) prior art lateral first drift region $217_a$ device, refer to above in FIG. **2**. To illustrate this, consider an example in which the $N^-$ region **11** has a doping of $1\times10^{14}$ ions $cm^{-3}$. The top gate layer **217** has an integrated doping of about $1\times10^{12}$ ions $cm^{-2}$ and is preferably not more than two microns thick while maintaining full breakdown. The thickness of the N and P layers **217**, **250** together is preferably less than ten microns and can be less than one micron. The same integrated doping in the $N^-$ body **11** requires a thickness of 100 microns. Thus, the N and P layers **217**, **250** respectively consume only a small fraction of the $N^-$ thickness required to provide doping equal to that portion of the N layer of the prior art device.

The lateral spacing between the drain contact $12_a$ and the channel $11_b$ in the device described above would be approximately 30 microns. In such a device, even if a full 100 micron thick $N^-$ body **11** were provided, it would have a higher resistance than the $N^-$ first drift region **217** provided according to the invention. This is because the average path length of current flowing from the drain contact **12A** down through the thick $N^-$ body **11** and back up to the surface edge of the channel at the drain-to-body junction would be greater than the direct path through the $N^-$ first drift region.

Maximum breakdown is achieved in the invention by providing doping densities of the N and P layers **217**, **250** such that they become totally depleted before breakdown is reached at any point along the junctions which they form with adjoining regions and before breakdown is reached at the junction between them. To insure that this occurs, the N region **217** should have an integrated doping not exceeding approximately $1\times10^{12}$ ions $cm^{-2}$ and the P region **250** should have a higher integrated doping not exceeding about 1.5 to $2\times10^{12}$ ions $cm^{-2}$.

To insure proper depletion of the P and N regions **250**, **217**, they must have the proper voltages applied. The N layer bias is achieved by connecting the N first drift region **217** to the higher concentration $N^+$ drain contact $12_a$ by overlapping the N first drift region **217** and drain contact $12_a$. The P region **250** bias is achieved by overlapping the P region **250** with the $P^-$ body **240** at least at one end of the channel, thereby applying the body voltage to the P layer **250**. This is illustrated in FIG. **12**.

With this structure and choice of doping levels, the desired results are achieved. When a reverse bias voltage is applied to the drain-to-body junction **15**, the same reverse bias appears on both the $PN^-$ junction **260** and the PN junction **270**. Depletion layers spread up into the N first drift region **217** and and down into the $N^-$ body **11** from the P layer **250**. In a preferred embodiment, the P and N first drift region dopings are chosen such that the N layer **217** becomes totally depleted at a lower voltage than that at which the P layer **250** becomes totally depleted. This insures that no residual undepleted portion of the N layer **217** is present which could reduce breakdown voltage.

As a result of the invention, the improved DMOS device provides a reduced resistance current path in the drain which does not depend on the $N^-$ doping. This allows the $N^-$ doping to be reduced to achieve a desired breakdown voltage with good manufacturing margin, while maintaining desirable low drift region resistance. In a multi-device process which includes LDMOS devices, the $N^-$ region can be adjusted to achieve the desired characteristics of one or more of the other device types, while the N first drift region **217** sets the drift region **217** resistance of the LDMOS.

Another embodiment of the DMOS invention is illustrated in FIG. **13**, where the N and P regions **217**, **221** are self-aligned to the gate **16** by using the gate **16** as a mask. An advantage of this structure is that N and P regions can be defined by the uncovered thin oxide area which extends from gate edge to overlap the drain contact. This embodiment requires no explicit mask step to delineate the location where the N and P regions are formed.

Still another embodiment, as illustrated in FIG. **14**, provides no gap between the $P^-$ body **240** and the P region **221** adjacent to the channel edge. The absence of the gap prevents current from flowing in the $N^-$ body **11**; so the entire drift region current path is in the N first drift region **217**. Elimination of the gap also allows the device structure to be made smaller. As with the other structure, the N and P regions may be self-aligned to the gate edge, as illustrated in FIG. **14**, or not self-aligned. They may also be covered by thick or thin oxide as a design option.

A preferred feature of the present invention provides that the body or substrate regions **11** shown in the FIGS. **3**, **4**, **6**, **7**, **8**, **9**, **11**, **13** and **14** are designed to be dielectrically or self-isolated regions. In contrast with the typical RESERF type of devices in which the bottom isolation junction plays a central role in the action of the device, the present invention contemplates that the isolation junction does not contribute to the depletion of the drift or top gate regions which are taught to be totally depleted. Prior art RESERF devices such as that described in U.S. Pat. No. 4,300,150 to Colak always require the substrate to be part of such depletion whereby the substrate must assume the most negative voltage in the device because of its role as one side of the isolation junction. As a result of this bias on the substrate or body region, the prior art RESERF type devices are susceptible to punch through from the device region through the epitaxial layer to the substrate. As a result of the present invention not having the substrate as part of the depletion mechanism, the invention can more effectively provide high voltage protection while not increasing the resistance of the channel path. Although the figures illustrate a nonisolating structure or self-isolated structure, it is understood that the invention applies equally well to dielectrically or junction isolated substrates.

While the present invention has been described with respect to several preferred manners of implementing the invention, it is to be understood that the claims appended hereto are intended to cover the invention in its broadest sense and are not to be limited to the specific implementations disclosed.

What is claimed is:

**1**. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said third semiconductor region;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said third semiconductor region;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body and material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said second and third semiconductor regions, and said fifth semiconductor region providing a second ON resistance in a second current flow path along the surface of said semiconductor body from said second semiconductor region through said channel and said fourth and fifth semiconductor regions to said third semiconductor region, so that said fifth semiconductor region serves to provide a current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said second and third semiconductor regions.

**2**. A semiconductor device according to claim **1**, wherein a peripheral edge of said gate electrode is aligned with a peripheral edge of said fifth semiconductor region.

**3**. A semiconductor device according to claim **1**, wherein said fourth semiconductor region overlaps said first semiconductor region.

**4**. A semiconductor device according to claim **1**, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

**5**. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said first conductivity type formed in a surface portion of said first semiconductor region and defining therewith a second PN junction, said second PN junction being spaced apart from said first PN junction by material of said first semiconductor region therebetween;

a third semiconductor region of said first conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof;

a fourth semiconductor region of said second conductivity type formed in said third surface portion of said semiconductor body and defining with said semiconductor body a third PN junction, said fourth semiconductor region being connected to said first semiconductor region and being contiguous with said first and third semiconductor regions;

a fifth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said fourth semiconductor region and defining therewith a fourth PN junction, said fifth semiconductor region being contiguous with said first and third semiconductor regions;

an insulator layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie material of said first and fourth semiconductor regions, that portion of said first semiconductor region lying beneath said gate electrode serving as a channel region of said device, said gate electrode having a gate voltage applied to induce a conductive channel through said first semiconductor region therebeneath; and wherein

when said device is reverse-biased, a first depletion region extends from said fourth PN junction into said fourth semiconductor region and said semiconductor body, and a second depletion region extends from said fifth PN junction into said fifth semicon-

ductor region and said fourth semiconductor region.

6. A semiconductor device according to claim 5, wherein the impurity concentration said fifth semiconductor region is such that said fifth semiconductor region is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said fourth semiconductor region.

7. A semiconductor device comprising:

a semiconductor body of a first conductivity type having a first surface;

a first semiconductor region of a second conductivity type formed in a first portion of said first surface of said semiconductor body, and defining a first PN junction with said semiconductor body;

a second semiconductor region of said second conductivity type formed in a second surface portion of said semiconductor body, spaced apart from said first surface portion by a third surface portion thereof and defining a second PN junction with said semiconductor body;

a third semiconductor region of said second conductivity type formed in a first surface part of said third surface portion of said semiconductor body spaced apart from said first surface portion of said semiconductor body by a second surface part of said third surface portion thereof and defining with said semiconductor body a third PN junction, said third semiconductor region being contiguous with said second semiconductor region;

a fourth semiconductor region of said first conductivity type, and having an impurity concentration greater than that of said semiconductor body, formed in said third semiconductor region and defining therewith a fourth PN junction;

an insulating layer formed on said first surface of said semiconductor body; and

a gate electrode formed on said insulator layer so as to overlie said second surface part of said third surface portion of said semiconductor body, that portion of said semiconductor body lying beneath said gate electrode serving as a channel region of said device, said gate electrode being applied with a gate voltage for inducing a conductive channel through said channel region;

said device being reverse-biased, so that a first depletion region extends from said third PN junction into said third semiconductor region and said semiconductor body and a second depletion region extends from said fourth PN junction into said third semiconductor region and said fourth semiconductor region;

said semiconductor body having a first ON resistance in a first current flow path therethrough between said first and second semiconductor regions, and said fourth semiconductor region providing a second ON resistance, less than said first ON resistance, in a second current flow path along the surface of said semiconductor body from said first semiconductor region through said channel and said third and fourth semiconductor regions to said second semiconductor region, so that said fourth semiconductor region serves to provide a reduced resistance current flow path in parallel with said first current flow path, thereby effectively reducing the total ON resistance of the overall current flow path between said first and second semiconductor regions; and

wherein the impurity concentration said fourth semiconductor region is such that said fourth semiconductor is completely depleted by said second depletion region at a reverse bias less than that at which said first and second depletion regions come together within and punch through said third semiconductor region.

8. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

an extended drain region of the second conductivity type extending laterally each way from said drain pocket to surface-adjoining positions,

a surface adjoining, top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

9. A high voltage MOS transistor according to claim 8, wherein said extended drain region has an impurity concentration greater than $1 \times 10^{12}$ cm$^{-2}$.

10. A high voltage MOS transistor according to claim 8, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor subscrate, said ohmic contact region overlapping said top layer of material.

11. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface,

a pair of laterally spaced source and drain pockets of semiconductor material of a second conductivity type within the substrate and adjoining the surface of said semiconductor material,

an extended drain region of the second conductivity type extending laterally from said drain pocket to a surface-adjoining position,

a surface adjoining top layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain pocket and said surface-adjoining position,

said top layer of material and said semiconductor material being subject to application of a reverse-bias voltage,

an insulating layer on the surface of said semiconductor material and covering at least that portion between the source pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from a semiconductor material re-

gion thereunder containing a channel that extends laterally between the source pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

**12**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region extends in a plurality of different directions from said drain pocket to respective plural surface adjoining positions.

**13**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region surrounds said drain pocket and extends to a surrounding surface adjoining position.

**14**. A high voltage MOS transistor according to claim **11**, wherein said drain pocket comprises a first relatively deep pocket of a first impurity concentration and a second relatively shallow pocket formed in a surface portion of said first relatively deep pocket and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

**15**. A high voltage MOS transistor according to claim **11**, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

**16**. A high voltage MOS transistor according to claim **11**, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top layer of material.

**17**. A high voltage field effect transistor device comprising:

semiconductor material of a first conductivity type having a surface;

a source region of a second conductivity type formed in a first surface portion of said semiconductor material;

a drain region of said second conductivity type formed in a second surface portion of said semiconductor material spaced apart from said first surface portion by a third surface portion therebetween;

an extended drain region of said second conductivity type extending from said drain region beneath a first portion of said third surface portion of said semiconductor material, to adjoin a second portion of said third surface portion of said semiconductor material, spaced apart from said said second surface portion of said semiconductor material, by said first portion of said third surface portion of said semiconductor material;

a surface region of said first conductivity type formed in said first portion of said third surface portion of said semiconductor material;

an insulating layer disposed on said surface of said semiconductor material, so as to overlie a third portion of said third surface portion of said semiconductor material between the second portion of said third surface portion of said semiconductor material and said first surface portion of said semiconductor material; and

a gate electrode disposed on that portion of said insulating layer overlying said third portion of said third surface portion of said semiconductor material, and wherein said surface region and said semiconductor material are subject to the application of a reverse bias voltage.

**18**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region extends laterally in a plurality of different directions from said drain region to adjoin said second portion of said third surface portion of said semiconductor material and to adjoin a fifth surface portion of said semiconductor material.

**19**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region surrounds said drain region and extends to a surrounding surface-adjoining portion of said semiconductor material.

**20**. A high voltage field effect transistor device according to claim **17**, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

**21**. A high voltage field effect transistor device according to claim **17**, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

**22**. A high voltage field effect transistor device according to claim **17**, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said surface region.

**23**. An integrated MOS/JFET transistor device comprising an insulated gate field effect transistor and a double-sided junction field effect transistor integrated together in semiconductor substrate which contains a source region, and a drain region, and a dual channel path formed in said semiconductor material between said source and drain regions, said dual channel path comprising an insulated gate-controlled channel region having a first conductivity type in the presence of a channel-inducing gate voltage, said insulated gate controlled channel region being contiguous with a double-sided junction channel region of said first conductivity type, and wherein said source region adjoins said insulated gate-controlled channel region and said drain region adjoins said double-sided channel region.

**24**. An integrated MOS/JFET transistor device according to claim **23**, wherein said insulated gate-controlled channel region comprises a surface portion of said semiconductor material adjoining said source region, and wherein said double-sided junction channel region comprises an extended drain region extending laterally from said drain region beneath a top gate region to said surface portion of said semiconductor material, an underlying portion of said semiconductor material extending beneath and adjoining said extended drain region and forming a bottom gate, said top gate region and said bottom gate forming respective PN junctions with said double-sided junction channel region.

**25**. An integrated MOS/JFET transistor device according to claim **23**, wherein said extended drain region and said double-sided junction channel region surround said drain region and extend to a surrounding surface-adjoining position.

**26**. An integrated MOS/JFET transistor device according to claim **23**, wherein said extended drain region and said double, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than

said first impurity concentration and providing a drain contact region.

27. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region and said double, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate.

28. An integrated MOS/JFET transistor device according to claim 23, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

29. A high voltage MOS transistor comprising:

semiconductor material of a first conductivity type having a surface;

source and drain regions of a second conductivity type adjoining spaced apart portions of the surface of said semiconductor material;

an extended drain region of said second conductivity type extending laterally from said drain region through said semiconductor material to a surface-adjoining portion of the surface of said semiconductor material;

a top gate semiconductor layer of said first conductivity type adjoining said drain region and adjoining said extended drain region along the surface of said semiconductor material to said surface-adjoining portion of the surface of said semiconductor material, said top gate semiconductor layer and said semiconductor material being subject to the application of a reverse-bias voltage;

an insulating layer on the surface of the semiconductor material and covering at least that portion of the surface of said semiconductor material between said source region and said surface-adjoining portion of said extended drain region; and

a gate electrode disposed on said insulating layer and being electrically isolated from that portion of the surface of said semiconductor material thereunder which forms a channel laterally between said source region and said surface-adjoining portion of said extended drain region, said gate electrode controlling, by field-effect, the flow of current thereunder through said channel.

30. A high voltage MOS transistor according to claim 29, wherein said extended drain region extends laterally each way from said drain region to surface-adjoining portions of the surface of said semiconductor material, and wherein said top gate semiconductor layer extends laterally in a plurality of different directions from said drain region and adjoins said extended drain region along the surface of said semiconductor material to said surface-adjoining portions of the surface of said semiconductor material.

31. A high voltage MOS transistor according to claim 29, wherein said extended drain region surrounds said drain region and extends to a surrounding surface adjoining position.

32. A high voltage MOS transistor according to claim 29, wherein said drain region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration and providing a drain contact region.

33. A high voltage MOS transistor according to claim 29, wherein said extended drain region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

34. A high voltage MOS transistor according to claim 29, further including an ohmic contact region of said first conductivity type formed in a surface adjoining portion of said semiconductor material, said ohmic contact region overlapping said top gate layer.

35. A high voltage diode comprising:

semiconductor material of a first conductivity type having a surface,

a first, surface-adjoining region of a second conductivity type;

a second surface-adjoining region of said first conductivity type spaced apart from said first, surface-adjoining region;

a third region of said second conductivity type extending laterally from said first, surface-adjoining region; and

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining region.

36. A high voltage diode according to claim 35, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

37. A high voltage diode according to claim 35, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

38. A high voltage diode according to claim 35, wherein said third region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

39. A lateral bipolar transistor having a high voltage base-collector diode comprising:

semiconductor material of a first conductivity type having a surface and forming a base of said bipolar transistor,

a first, surface-adjoining collector region of a second conductivity type forming a base-collector junction with said semiconductor material;

a second surface-adjoining base region of said first conductivity type spaced apart from said first, surface-adjoining collector region;

a third, extended collector region of said second conductivity type extending laterally from said first, surface-adjoining collector region, so that said base-collector junction extends laterally from said first, surface adjoining collector region;

a fourth, surface-adjoining region of said first conductivity type overlying an intermediate portion of said third, laterally extending and surface-adjoining extended collector region; and

a fifth, surface-adjoining emitter region of said second conductivity type formed in said second surface-adjoining base region and defining therewith an emitter-base junction.

40. A lateral bipolar transistor according to claim 39, wherein said third region surrounds said first, surface-adjoining region and extends to a surrounding surface adjoining position.

41. A lateral bipolar transistor according to claim 39, wherein said first region comprises a first relatively deep region of a first impurity concentration and a second relatively shallow region formed in a surface portion of said first relatively deep region and having a second impurity concentration greater than said first impurity concentration.

42. A lateral bipolar transistor according to claim 39, wherein said third, extended collector region has an impurity concentration greater than $1\times10^{12}$ $cm^{-2}$.

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Additional name(s) attached? ☐ Yes ■ No

2. Name and address of receiving party(ies):
**Intersil Corporation**
**2401 Palm Bay Road, N.E.**
**Palm Bay, FL 32905**

Additional names/addresses attached? ☐ Yes ■ No

3. Nature of conveyance:
- ■ Assignment
- ☐ Merger
- ☐ Security Agreement
- ☐ Change of Name
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Execution Date: **August 13, 1999**

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5. Name/address of party to whom correspondence concerning document should be mailed:

**Timothy A. French**
**Fish & Richardson P.C.**
**225 Franklin Street**
**Boston, MA 02110-2804**

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I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Susanne McNeill

# HARRIS PATENT ASSIGNMENT

FOR VALUE RECEIVED, the receipt and sufficiency of which is hereby acknowledged, the undersigned Harris Corporation, a corporation of Delaware having a place of business at 1025 West NASA Blvd., Melbourne, Florida 32919 ("Harris"), does hereby assign, transfer and set over to Intersil Corporation, a corporation of Delaware having a place of business at 2401 Palm Bay Road, N.E., Melbourne, Florida 32905, its successors, legal representatives and assigns (hereinafter "Assignee") the entire right, title and interest in and to each of the United States patents and patent applications listed in the attached Appendix A, together with the inventions disclosed and/or claimed therein, as well as all applications for patent and any Letters Patent which may be granted therefor, in the United States of America and in all foreign countries, and in and to any and all divisions, continuations, continuations-in-part of said applications, or re-issues or extensions of said patents or Letters Patent, and all rights under the International Convention for the Protection of Industrial Property and similar agreements (hereinafter individually and collectively "Patents").

Harris hereby appoints Assignee as its agent and attorney-in-fact to conduct all business before the United States Patent & Trademark Office and the patent offices in all foreign countries in the name of Harris in connection with said Patents.

Harris hereby authorizes and requests that the United States Patent & Trademark Office, and the patent offices of all foreign countries, to issue any and all Letters Patent of the United States and patents in all foreign countries resulting from said application or any division or divisions or continuing applications thereof in the United States and all foreign countries to Assignee, as assignee of the entire interest, and Harris hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed and will not execute, any agreement in conflict herewith.

Harris further agrees to cooperate with the Assignee in every way possible and to do all affirmative acts, and to execute all papers which counsel for Assignee shall advise are necessary and/or desirable without charge to Assignee in connection with said Patents including, without limitation, the execution of separate assignments for filing in the United States Patent & Trademark Office and the patent offices of all foreign countries in connection with said Patents.

The undersigned Harris hereby grants to Howard Rothman; John DeAngelis, Reg. No. 30,622; Ferdinand M. Romano, Reg. No. 32,752; and L. Lawton Rogers, III, Reg. No. 24,302 the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent Office for recordation of this document.

IN WITNESS WHEREOF,

Date August 13, 1999

HARRIS CORPORATION

By: Scott T. Mikuen (Signature)

Scott T. Mikuen (Printed Name)

Assistant Secretary (Title)

ATTEST:

[SEAL]

Date August 13, 1999

Secretary

# APPENDIX A
# HARRIS CORPORATION
# ISSUED PATENTS

| Patent Number | Issue Date |
|---|---|
| 4236231 | 25-Nov-1980 |
| 4260431 | 07-Apr-1981 |
| 4272833 | 09-Jun-1981 |
| 4281449 | 04-Aug-1981 |
| 4283236 | 11-Aug-1981 |
| 4288911 | 15-Sep-1981 |
| 4290831 | 22-Sep-1981 |
| 4292730 | 06-Oct-1981 |
| 4299024 | 10-Nov-1981 |
| 4301383 | 17-Nov-1981 |
| 4305106 | 08-Dec-1981 |
| 4309813 | 12-Jan-1982 |
| 4312046 | 19-Jan-1982 |
| 4319257 | 09-Mar-1982 |
| 4334646 | 15-Jun-1982 |
| 4368395 | 11-Jan-1983 |
| 4380710 | 19-Apr-1983 |
| 4389721 | 21-Jun-1983 |
| 4398142 | 09-Aug-1983 |
| 4401940 | 30-Aug-1983 |
| 4402002 | 30-Aug-1983 |
| 4402065 | 30-Aug-1983 |
| 4403399 | 13-Sep-1983 |
| 4409686 | 11-Oct-1983 |
| 4420766 | 13-Dec-1983 |
| 4446444 | 01-May-1984 |
| 4450414 | 22-May-1984 |
| 4454432 | 12-Jun-1984 |
| 4456918 | 26-Jun-1984 |
| 4461000 | 17-Jul-1984 |
| 4462020 | 24-Jul-1984 |
| 4464631 | 07-Aug-1984 |
| 4464825 | 14-Aug-1984 |
| 4466179 | 21-Aug-1984 |
| 4468414 | 28-Aug-1984 |
| 4471236 | 11-Sep-1984 |
| 4471376 | 11-Sep-1984 |
| 4472648 | 18-Sep-1984 |
| 4480219 | 30-Oct-1984 |
| 4495537 | 22-Jan-1985 |
| 4495694 | 29-Jan-1985 |
| 4503387 | 05-Mar-1985 |
| 4514802 | 30-Apr-1985 |
| 4524246 | 18-Jun-1985 |
| 4528461 | 09-Jul-1985 |
| 4528462 | 09-Jul-1985 |
| 4528504 | 09-Jul-1985 |
| 4532003 | 30-Jul-1985 |
| 4532481 | 30-Jul-1985 |
| 4536231 | 20-Aug-1985 |
| 4546539 | 15-Oct-1985 |
| 4554059 | 19-Nov-1985 |
| 4559608 | 17-Dec-1985 |

| Patent Number | Issue Date |
|---|---|
| 4560948 | 24-Dec-1985 |
| 4566796 | 28-Jan-1986 |
| 4567385 | 28-Jan-1986 |
| 4567578 | 28-Jan-1986 |
| 4578859 | 01-Apr-1986 |
| 4580131 | 01-Apr-1986 |
| 4581548 | 08-Apr-1986 |
| 4584660 | 22-Apr-1986 |
| 4586193 | 29-Apr-1986 |
| 4590664 | 27-May-1986 |
| 4591826 | 27-May-1986 |
| 4594265 | 10-Jun-1986 |
| 4595608 | 17-Jun-1986 |
| 4596068 | 24-Jun-1986 |
| 4599789 | 15-Jul-1986 |
| 4606936 | 19-Aug-1986 |
| 4608530 | 26-Aug-1986 |
| 4613772 | 23-Sep-1986 |
| 4616178 | 07-Oct-1986 |
| 4618743 | 21-Oct-1986 |
| 4620179 | 28-Oct-1986 |
| 4624749 | 25-Nov-1986 |
| 4631636 | 23-Dec-1986 |
| 4632557 | 30-Dec-1986 |
| 4633107 | 30-Dec-1986 |
| 4636743 | 13-Jan-1987 |
| 4636744 | 13-Jan-1987 |
| 4639684 | 27-Jan-1987 |
| 4639896 | 27-Jan-1987 |
| 4644191 | 17-Feb-1987 |
| 4644192 | 17-Feb-1987 |
| 4644383 | 17-Feb-1987 |
| 4650696 | 17-Mar-1987 |
| 4652895 | 24-Mar-1987 |
| 4658253 | 14-Apr-1987 |
| 4665327 | 12-May-1987 |
| 4665425 | 12-May-1987 |
| 4666737 | 19-May-1987 |
| 4669884 | 02-Jun-1987 |
| 4670769 | 02-Jun-1987 |
| 4675798 | 23-Jun-1987 |
| 4677321 | 30-Jun-1987 |
| 4682057 | 21-Jul-1987 |
| 4682059 | 21-Jul-1987 |
| 4683485 | 28-Jul-1987 |
| 4684055 | 04-Aug-1987 |
| 4686384 | 11-Aug-1987 |
| 4694313 | 15-Sep-1987 |
| 4698589 | 06-Oct-1987 |
| 4701644 | 20-Oct-1987 |
| 4702000 | 27-Oct-1987 |
| 4702967 | 27-Oct-1987 |
| 4703505 | 27-Oct-1987 |
| 4703566 | 03-Nov-1987 |
| 4705596 | 10-Nov-1987 |
| 4705597 | 10-Nov-1987 |
| 4708747 | 24-Nov-1987 |
| 4713260 | 15-Dec-1987 |

58

| Patent Number | Issue Date |
|---|---|
| 4713681 | 15-Dec-1987 |
| 4716071 | 29-Dec-1987 |
| 4717680 | 05-Jan-1988 |
| 4717847 | 05-Jan-1988 |
| 4719598 | 12-Jan-1988 |
| 4720739 | 19-Jan-1988 |
| 4728820 | 01-Mar-1988 |
| 4729008 | 01-Mar-1988 |
| 4733168 | 22-Mar-1988 |
| 4734885 | 29-Mar-1988 |
| 4734886 | 29-Mar-1988 |
| 4752591 | 21-Jun-1988 |
| 4753851 | 28-Jun-1988 |
| 4754388 | 28-Jun-1988 |
| 4755770 | 05-Jul-1988 |
| 4757363 | 12-Jul-1988 |
| 4757528 | 12-Jul-1988 |
| 4760433 | 26-Jul-1988 |
| 4761570 | 02-Aug-1988 |
| 4771016 | 13-Sep-1988 |
| 4780688 | 25-Oct-1988 |
| 4781853 | 01-Nov-1988 |
| 4783637 | 08-Nov-1988 |
| 4786608 | 22-Nov-1988 |
| 4789426 | 06-Dec-1988 |
| 4795718 | 03-Jan-1989 |
| 4801065 | 31-Jan-1989 |
| 4804865 | 14-Feb-1989 |
| 4807012 | 21-Feb-1989 |
| 4808547 | 28-Feb-1989 |
| 4812962 | 14-Mar-1989 |
| 4814285 | 21-Mar-1989 |
| 4818725 | 04-Apr-1989 |
| 4818901 | 04-Apr-1989 |
| 4820968 | 11-Apr-1989 |
| 4823173 | 18-Apr-1989 |
| 4823300 | 18-Apr-1989 |
| 4839711 | 13-Jun-1989 |
| 4845052 | 04-Jul-1989 |
| 4851078 | 25-Jul-1989 |
| 4851257 | 25-Jul-1989 |
| 4854986 | 08-Aug-1989 |
| 4855625 | 08-Aug-1989 |
| 4857764 | 15-Aug-1989 |
| 4859280 | 22-Aug-1989 |
| 4862231 | 29-Aug-1989 |
| 4868778 | 19-Sep-1989 |
| 4873564 | 10-Oct-1989 |
| 4876579 | 24-Oct-1989 |
| 4879520 | 07-Nov-1989 |
| 4879523 | 07-Nov-1989 |
| 4881111 | 14-Nov-1989 |
| 4882698 | 21-Nov-1989 |
| 4888741 | 19-Dec-1989 |
| 4891604 | 02-Jan-1990 |
| 4891606 | 02-Jan-1990 |
| 4893088 | 09-Jan-1990 |
| 4897362 | 30-Jan-1990 |

| Patent Number | Issue Date |
|---|---|
| 4897366 | 30-Jan-1990 |
| 4897567 | 30-Jan-1990 |
| 4900689 | 13-Feb-1990 |
| 4908566 | 13-Mar-1990 |
| 4908683 | 13-Mar-1990 |
| 4912053 | 27-Mar-1990 |
| 4914501 | 03-Apr-1990 |
| 4916497 | 10-Apr-1990 |
| 4923820 | 08-May-1990 |
| 4923826 | 08-May-1990 |
| 4927777 | 22-May-1990 |
| 4929566 | 29-May-1990 |
| 4929568 | 29-May-1990 |
| 4929923 | 29-May-1990 |
| 4937774 | 26-Jun-1990 |
| 4941027 | 10-Jul-1990 |
| 4945070 | 31-Jul-1990 |
| 4945262 | 31-Jul-1990 |
| 4948746 | 14-Aug-1990 |
| 4949296 | 14-Aug-1990 |
| 4951102 | 21-Aug-1990 |
| 4956306 | 11-Sep-1990 |
| 4968628 | 06-Nov-1990 |
| 4968900 | 06-Nov-1990 |
| 4970573 | 13-Nov-1990 |
| 4970677 | 13-Nov-1990 |
| 4975751 | 04-Dec-1990 |
| 4978868 | 18-Dec-1990 |
| 4978925 | 18-Dec-1990 |
| 4979011 | 18-Dec-1990 |
| 4980651 | 25-Dec-1990 |
| 4982194 | 01-Jan-1991 |
| 4988902 | 29-Jan-1991 |
| 5008719 | 16-Apr-1991 |
| 5010377 | 23-Apr-1991 |
| 5014055 | 07-May-1991 |
| 5014108 | 07-May-1991 |
| 5015877 | 14-May-1991 |
| 5015887 | 14-May-1991 |
| 5021359 | 04-Jun-1991 |
| 5028824 | 02-Jul-1991 |
| 5028973 | 02-Jul-1991 |
| 5030862 | 09-Jul-1991 |
| 5032529 | 16-Jul-1991 |
| 5034343 | 23-Jul-1991 |
| 5034789 | 23-Jul-1991 |
| 5036219 | 30-Jul-1991 |
| 5037765 | 06-Aug-1991 |
| 5038248 | 06-Aug-1991 |
| 5039888 | 13-Aug-1991 |
| 5047974 | 10-Sep-1991 |
| 5051619 | 24-Sep-1991 |
| 5051949 | 24-Sep-1991 |
| 5053345 | 01-Oct-1991 |
| 5053353 | 01-Oct-1991 |
| 5057895 | 15-Oct-1991 |
| 5059982 | 22-Oct-1991 |
| 5060192 | 22-Oct-1991 |

| Patent Number | Issue Date |
|---|---|
| 5066995 | 19-Nov-1991 |
| 5070388 | 03-Dec-1991 |
| 5070451 | 03-Dec-1991 |
| 5070596 | 10-Dec-1991 |
| 5079176 | 07-Jan-1992 |
| 5079608 | 07-Jan-1992 |
| 5079734 | 07-Jan-1992 |
| 5081061 | 14-Jan-1992 |
| 5081063 | 14-Jan-1992 |
| 5081410 | 14-Jan-1992 |
| 5084839 | 28-Jan-1992 |
| 5085084 | 04-Feb-1992 |
| 5086242 | 04-Feb-1992 |
| 5091331 | 25-Feb-1992 |
| 5091336 | 25-Feb-1992 |
| 5095343 | 10-Mar-1992 |
| 5096850 | 17-Mar-1992 |
| 5097319 | 17-Mar-1992 |
| 5105099 | 14-Apr-1992 |
| 5107312 | 21-Apr-1992 |
| 5111268 | 05-May-1992 |
| 5113361 | 12-May-1992 |
| 5117282 | 26-May-1992 |
| 5118632 | 02-Jun-1992 |
| 5119321 | 02-Jun-1992 |
| 5120669 | 09-Jun-1992 |
| 5130569 | 14-Jul-1992 |
| 5134321 | 28-Jul-1992 |
| 5138319 | 11-Aug-1992 |
| 5138413 | 11-Aug-1992 |
| 5140326 | 18-Aug-1992 |
| 5142244 | 25-Aug-1992 |
| 5148475 | 15-Sep-1992 |
| 5150120 | 22-Sep-1992 |
| 5151953 | 29-Sep-1992 |
| 5164802 | 17-Nov-1992 |
| 5184128 | 02-Feb-1993 |
| 5185292 | 09-Feb-1993 |
| 5194867 | 16-Mar-1993 |
| 5196373 | 23-Mar-1993 |
| 5196737 | 23-Mar-1993 |
| 5198385 | 30-Mar-1993 |
| 5200733 | 06-Apr-1993 |
| 5206821 | 27-Apr-1993 |
| 5214329 | 25-May-1993 |
| 5217919 | 08-Jun-1993 |
| 5218213 | 08-Jun-1993 |
| 5218220 | 08-Jun-1993 |
| 5218321 | 08-Jun-1993 |
| 5220868 | 22-Jun-1993 |
| 5228192 | 20-Jul-1993 |
| 5228330 | 20-Jul-1993 |
| 5229661 | 20-Jul-1993 |
| 5233289 | 03-Aug-1993 |
| 5235205 | 10-Aug-1993 |
| 5240876 | 31-Aug-1993 |
| 5241213 | 31-Aug-1993 |
| 5243211 | 07-Sep-1993 |

| Patent Number | Issue Date |
|---|---|
| 5247199 | 21-Sep-1993 |
| 5248894 | 28-Sep-1993 |
| 5248901 | 28-Sep-1993 |
| 5248932 | 28-Sep-1993 |
| 5258939 | 02-Nov-1993 |
| 5260590 | 09-Nov-1993 |
| 5262689 | 16-Nov-1993 |
| 5262976 | 16-Nov-1993 |
| 5264719 | 23-Nov-1993 |
| 5265225 | 23-Nov-1993 |
| 5266135 | 30-Nov-1993 |
| 5270265 | 14-Dec-1993 |
| 5270569 | 14-Dec-1993 |
| 5272104 | 21-Dec-1993 |
| 5276633 | 04-Jan-1994 |
| 5279850 | 18-Jan-1994 |
| 5283461 | 01-Feb-1994 |
| 5287068 | 15-Feb-1994 |
| 5287071 | 15-Feb-1994 |
| 5289336 | 22-Feb-1994 |
| 5293052 | 08-Mar-1994 |
| 5298434 | 29-Mar-1994 |
| 5300877 | 05-Apr-1994 |
| 5302859 | 12-Apr-1994 |
| 5306650 | 26-Apr-1994 |
| 5306944 | 26-Apr-1994 |
| 5307023 | 26-Apr-1994 |
| 5311054 | 10-May-1994 |
| 5311070 | 10-May-1994 |
| 5312262 | 17-May-1994 |
| 5315144 | 24-May-1994 |
| 5317184 | 31-May-1994 |
| 5319757 | 07-Jun-1994 |
| 5322804 | 21-Jun-1994 |
| 5323036 | 21-Jun-1994 |
| 5327006 | 05-Jul-1994 |
| 5329187 | 12-Jul-1994 |
| 5332931 | 26-Jul-1994 |
| 5334273 | 02-Aug-1994 |
| 5334929 | 02-Aug-1994 |
| 5335132 | 02-Aug-1994 |
| 5338960 | 16-Aug-1994 |
| 5341009 | 23-Aug-1994 |
| 5341335 | 23-Aug-1994 |
| 5345236 | 06-Sep-1994 |
| 5347169 | 13-Sep-1994 |
| 5350935 | 27-Sep-1994 |
| 5352327 | 04-Oct-1994 |
| 5357089 | 18-Oct-1994 |
| 5359211 | 25-Oct-1994 |
| 5359236 | 25-Oct-1994 |
| 5362667 | 08-Nov-1994 |
| 5366932 | 22-Nov-1994 |
| 5367211 | 22-Nov-1994 |
| 5369309 | 29-Nov-1994 |
| 5370568 | 06-Dec-1994 |
| 5373183 | 13-Dec-1994 |
| 5382541 | 17-Jan-1995 |

56

| Patent Number | Issue Date |
|---|---|
| 5382825 | 17-Jan-1995 |
| 5382916 | 17-Jan-1995 |
| 5387555 | 07-Feb-1995 |
| 5391903 | 21-Feb-1995 |
| 5395774 | 07-Mar-1995 |
| 5397714 | 14-Mar-1995 |
| 5399892 | 21-Mar-1995 |
| 5406223 | 11-Apr-1995 |
| 5416351 | 16-May-1995 |
| 5418002 | 23-May-1995 |
| 5420499 | 30-May-1995 |
| 5422288 | 06-Jun-1995 |
| 5423889 | 13-Jun-1995 |
| 5424563 | 13-Jun-1995 |
| 5428492 | 27-Jun-1995 |
| 5429958 | 04-Jul-1995 |
| 5429993 | 04-Jul-1995 |
| 5434357 | 18-Jul-1995 |
| 5436189 | 25-Jul-1995 |
| 5438221 | 01-Aug-1995 |
| 5440506 | 08-Aug-1995 |
| 5446316 | 29-Aug-1995 |
| 5446368 | 29-Aug-1995 |
| 5448100 | 05-Sep-1995 |
| 5448102 | 05-Sep-1995 |
| 5450326 | 12-Sep-1995 |
| 5450339 | 12-Sep-1995 |
| 5451263 | 19-Sep-1995 |
| 5455442 | 03-Oct-1995 |
| 5455782 | 03-Oct-1995 |
| 5463344 | 31-Oct-1995 |
| 5466963 | 14-Nov-1995 |
| 5468668 | 21-Nov-1995 |
| 5469556 | 21-Nov-1995 |
| 5471131 | 28-Nov-1995 |
| 5473193 | 05-Dec-1995 |
| 5481129 | 02-Jan-1996 |
| 5493207 | 20-Feb-1996 |
| 5493581 | 20-Feb-1996 |
| 5497013 | 05-Mar-1996 |
| 5504033 | 02-Apr-1996 |
| 5504449 | 02-Apr-1996 |
| 5508551 | 16-Apr-1996 |
| 5515402 | 07-May-1996 |
| 5515417 | 07-May-1996 |
| 5515434 | 07-May-1996 |
| 5516625 | 14-May-1996 |
| 5517047 | 14-May-1996 |
| 5517058 | 14-May-1996 |
| 5517565 | 14-May-1996 |
| 5519732 | 21-May-1996 |
| 5521436 | 28-May-1996 |
| 5525869 | 11-Jun-1996 |
| 5526392 | 11-Jun-1996 |
| 5526768 | 18-Jun-1996 |
| 5528682 | 18-Jun-1996 |
| 5532635 | 02-Jul-1996 |
| 5539707 | 23-Jul-1996 |

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| Patent Number | Issue Date |
|---|---|
| 5541435 | 30-Jul-1996 |
| 5541538 | 30-Jul-1996 |
| 5544095 | 06-Aug-1996 |
| 5546038 | 13-Aug-1996 |
| 5547896 | 20-Aug-1996 |
| 5548542 | 20-Aug-1996 |
| 5552345 | 03-Sep-1996 |
| 5557175 | 17-Sep-1996 |
| 5561303 | 01-Oct-1996 |
| 5561607 | 01-Oct-1996 |
| 5563834 | 08-Oct-1996 |
| 5567978 | 22-Oct-1996 |
| 5569620 | 29-Oct-1996 |
| 5569957 | 29-Oct-1996 |
| 5570392 | 29-Oct-1996 |
| 5570407 | 29-Oct-1996 |
| 5572161 | 05-Nov-1996 |
| 5572162 | 05-Nov-1996 |
| 5574572 | 12-Nov-1996 |
| 5574609 | 12-Nov-1996 |
| 5574618 | 12-Nov-1996 |
| 5574671 | 12-Nov-1996 |
| 5576654 | 19-Nov-1996 |
| 5576695 | 19-Nov-1996 |
| 5577656 | 26-Nov-1996 |
| 5580816 | 03-Dec-1996 |
| 5581444 | 03-Dec-1996 |
| 5581475 | 03-Dec-1996 |
| 5583442 | 10-Dec-1996 |
| 5585310 | 17-Dec-1996 |
| 5585661 | 17-Dec-1996 |
| 5586072 | 17-Dec-1996 |
| 5587103 | 24-Dec-1996 |
| 5594261 | 14-Jan-1997 |
| 5598157 | 28-Jan-1997 |
| 5602052 | 11-Feb-1997 |
| 5602054 | 11-Feb-1997 |
| 5603779 | 18-Feb-1997 |
| 5606288 | 25-Feb-1997 |
| 5608259 | 04-Mar-1997 |
| 5608264 | 04-Mar-1997 |
| 5610093 | 11-Mar-1997 |
| 5610792 | 11-Mar-1997 |
| 5614422 | 25-Mar-1997 |
| 5614852 | 25-Mar-1997 |
| 5614867 | 25-Mar-1997 |
| 5617090 | 01-Apr-1997 |
| 5617344 | 01-Apr-1997 |
| 5617473 | 01-Apr-1997 |
| 5618752 | 08-Apr-1997 |
| 5619270 | 08-Apr-1997 |
| 5621307 | 15-Apr-1997 |
| 5621355 | 15-Apr-1997 |
| 5621477 | 15-Apr-1997 |
| 5621478 | 15-Apr-1997 |
| 5622878 | 22-Apr-1997 |
| 5622890 | 22-Apr-1997 |
| 5625566 | 29-Apr-1997 |

| Patent Number | Issue Date |
|---|---|
| 5627489 | 06-May-1997 |
| 5631599 | 20-May-1997 |
| 5633180 | 27-May-1997 |
| 5633815 | 27-May-1997 |
| 5636274 | 03-Jun-1997 |
| 5637908 | 10-Jun-1997 |
| 5639688 | 17-Jun-1997 |
| 5640300 | 17-Jun-1997 |
| 5640346 | 17-Jun-1997 |
| 5642247 | 24-Jun-1997 |
| 5643821 | 01-Jul-1997 |
| 5644309 | 01-Jul-1997 |
| 5646067 | 08-Jul-1997 |
| 5648678 | 15-Jul-1997 |
| 5649009 | 15-Jul-1997 |
| 5650344 | 22-Jul-1997 |
| 5650639 | 22-Jul-1997 |
| 5650658 | 22-Jul-1997 |
| 5650971 | 22-Jul-1997 |
| 5652153 | 29-Jul-1997 |
| 5654226 | 05-Aug-1997 |
| 5654662 | 05-Aug-1997 |
| 5654991 | 05-Aug-1997 |
| 5656512 | 12-Aug-1997 |
| 5659261 | 19-Aug-1997 |
| 5659269 | 19-Aug-1997 |
| 5659570 | 19-Aug-1997 |
| 5661736 | 26-Aug-1997 |
| 5663860 | 02-Sep-1997 |
| 5665634 | 09-Sep-1997 |
| 5666083 | 09-Sep-1997 |
| 5668397 | 16-Sep-1997 |
| 5668409 | 16-Sep-1997 |
| 5668468 | 16-Sep-1997 |
| 5669599 | 23-Sep-1997 |
| 5670413 | 23-Sep-1997 |
| 5670799 | 23-Sep-1997 |
| 5671272 | 23-Sep-1997 |
| 5672998 | 30-Sep-1997 |
| 5675281 | 07-Oct-1997 |
| 5675339 | 07-Oct-1997 |
| 5677599 | 14-Oct-1997 |
| 5678030 | 14-Oct-1997 |
| 5680072 | 21-Oct-1997 |
| 5682062 | 28-Oct-1997 |
| 5682111 | 28-Oct-1997 |
| 5682336 | 28-Oct-1997 |
| 5683075 | 04-Nov-1997 |
| 5683939 | 04-Nov-1997 |
| 5684305 | 04-Nov-1997 |
| 5686322 | 11-Nov-1997 |
| 5686822 | 11-Nov-1997 |
| 5689129 | 18-Nov-1997 |
| 5694417 | 02-Dec-1997 |
| 5696452 | 09-Dec-1997 |
| 5701097 | 23-Dec-1997 |
| 5708549 | 13-Jan-1998 |
| 5712870 | 27-Jan-1998 |

| Patent Number | Issue Date |
|---|---|
| 5717243 | 10-Feb-1998 |
| 5717322 | 10-Feb-1998 |
| 5717617 | 10-Feb-1998 |
| 5717736 | 10-Feb-1998 |
| 5719326 | 17-Feb-1998 |
| 5724370 | 03-Mar-1998 |
| 5728624 | 17-Mar-1998 |
| 5729038 | 17-Mar-1998 |
| 5732105 | 24-Mar-1998 |
| 5736885 | 07-Apr-1998 |
| 5736903 | 07-Apr-1998 |
| 5742204 | 21-Apr-1998 |
| 5744851 | 28-Apr-1998 |
| 5744852 | 28-Apr-1998 |
| 5745563 | 28-Apr-1998 |
| 5750432 | 12-May-1998 |
| 5757036 | 26-May-1998 |
| 5757794 | 26-May-1998 |
| 5764113 | 09-Jun-1998 |
| 5767740 | 16-Jun-1998 |
| 5767757 | 16-Jun-1998 |
| 5770878 | 23-Jun-1998 |
| 5770880 | 23-Jun-1998 |
| 5771012 | 23-Jun-1998 |
| 5773151 | 30-Jun-1998 |
| 5773891 | 30-Jun-1998 |
| 5776814 | 07-Jul-1998 |
| 5777346 | 07-Jul-1998 |
| 5777362 | 07-Jul-1998 |
| 5780311 | 14-Jun-1998 |
| 5782975 | 21-Jul-1998 |
| 5789949 | 04-Aug-1998 |
| 5789982 | 04-Aug-1998 |
| 5790060 | 04-Aug-1998 |
| 5793193 | 11-Aug-1998 |
| 5798557 | 25-Aug-1998 |
| 5798724 | 29-Aug-1998 |
| 5801084 | 01-Sep-1998 |
| 5804846 | 08-Sep-1998 |
| 5805020 | 08-Sep-1998 |
| 5807780 | 15-Sep-1998 |
| 5807783 | 15-Sep-1998 |
| 5808348 | 15-Sep-1998 |
| 5808353 | 15-Sep-1998 |
| 5808489 | 15-Sep-1998 |
| 5808883 | 15-Sep-1998 |
| 5809410 | 15-Sep-1998 |
| 5812029 | 22-Sep-1998 |
| 5812658 | 22-Sep-1998 |
| 5814889 | 29-Sep-1998 |
| 5817564 | 06-Oct-1998 |
| 5821740 | 13-Oct-1998 |
| 5825092 | 20-Oct-1998 |
| 5830048 | 03-Nov-1998 |
| 5830279 | 03-Nov-1998 |
| 5831423 | 03-Nov-1998 |
| 5833758 | 10-Nov-1998 |
| 5837553 | 17-Nov-1998 |

| Patent Number | Issue Date |
|---|---|
| 5837603 | 17-Nov-1998 |
| 5841169 | 24-Nov-1998 |
| 5841182 | 24-Nov-1998 |
| 5841324 | 24-Nov-1998 |
| 5849627 | 15-Dec-1998 |
| 5851864 | 22-Dec-1998 |
| 5856695 | 05-Jan-1999 |
| 5856700 | 05-Jan-1999 |
| 5856742 | 05-Jan-1999 |
| 5861826 | 19-Jan-1999 |
| 5870266 | 09-Feb-1999 |
| 5872028 | 16-Feb-1999 |
| 5872044 | 16-Feb-1999 |
| 5877041 | 02-Mar-1999 |
| 5877044 | 02-Mar-1999 |
| 5880513 | 09-Mar-1999 |
| 5882423 | 16-Mar-1999 |
| 5883414 | 16-Mar-1999 |
| 5883565 | 16-Mar-1999 |
| 5883921 | 16-Mar-1999 |
| 5892223 | 06-Apr-1999 |
| 5892264 | 06-Apr-1999 |
| 5892375 | 06-Apr-1999 |
| 5892472 | 06-Apr-1999 |
| 5894141 | 13-Apr-1999 |
| 5895953 | 20-Apr-1999 |
| 5896053 | 20-Apr-1999 |
| 5900643 | 04-May-1999 |
| 5913130 | 15-Jun-1999 |
| 5914280 | 22-Jun-1999 |
| 5915168 | 22-Jun-1999 |
| 5920108 | 06-Jul-1999 |
| 5920219 | 06-Jul-1999 |
| 5920224 | 06-Jul-1999 |
| 5920452 | 06-Jul-1999 |
| 5923207 | 13-Jul-1999 |
| 5923209 | 13-Jul-1999 |
| B1 5051619 | 02-Mar-1993 |

# PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

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|---|---|
| SUBMISSION TYPE: | NEW ASSIGNMENT |
| NATURE OF CONVEYANCE: | CHANGE OF NAME |

CONVEYING PARTY DATA

| Name | Execution Date |
|---|---|
| INTERSIL CORPORATION | 05/25/2001 |

RECEIVING PARTY DATA

| | |
|---|---|
| Name: | INTERSIL COMMUNICATIONS, INC. |
| Street Address: | 1001 Murphy Ranch Road |
| City: | Milpitas |
| State/Country: | CALIFORNIA |
| Postal Code: | 95035 |

PROPERTY NUMBERS Total: 2

| Property Type | Number |
|---|---|
| Patent Number: | 4823173 |
| Patent Number: | 5264719 |

CH $80.00 4823173

CORRESPONDENCE DATA

Fax Number: (703)931-6037
*Correspondence will be sent via US Mail when the fax attempt is unsuccessful.*
Phone: 2022363707
Email: wgwalter@aol.com
Correspondent Name: Wallace G. Walter
Address Line 1: 5726 Clarence Ave
Address Line 4: Alexandria, VIRGINIA 22311

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|---|---|
| NAME OF SUBMITTER: | Wallace G. Walter |

Total Attachments: 4
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source=IntersilNameChange#page3.tif
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# Delaware

PAGE 1

*The First State*

I, HARRIET SMITH WINDSOR, SECRETARY OF STATE OF THE STATE OF DELAWARE, DO HEREBY CERTIFY THE ATTACHED IS A TRUE AND CORRECT COPY OF THE RESTATED CERTIFICATE OF "INTERSIL CORPORATION", CHANGING ITS NAME FROM "INTERSIL CORPORATION" TO "INTERSIL COMMUNICATIONS, INC.", FILED IN THIS OFFICE ON THE TWENTY-FIFTH DAY OF MAY, A.D. 2001, AT 4:15 O'CLOCK P.M.

Harriet Smith Windsor

3050122 8100

050839147

DATE: 10-13-05

# AMENDED AND RESTATED CERTIFICATE OF INCORPORATION
# OF
# INTERSIL CORPORATION

INTERSIL CORPORATION, a corporation organized and existing under the laws of the State of Delaware, hereby certifies as follows:

FIRST: The present name of the corporation is INTERSIL CORPORATION and the name under which the corporation was originally incorporated is HSS Operating Corporation. The date of filing of its original Certificate of Incorporation with the Secretary of State of the State of Delaware was June 2, 1999.

SECOND: This Amended and Restated Certificate of Incorporation (the "Certificate") restates and integrates and further amends in its entirety the Certificate of Incorporation of this corporation. This Certificate was duly adopted by a majority vote of the stockholders of the corporation in accordance with Sections 228, 242 and 245 of the General Corporation Law of the State of Delaware.

THIRD: This Certificate shall become effective immediately upon its filing with the Secretary of State of the State of Delaware.

FOURTH: Upon the filing of the Certificate with the Secretary of State of the State of Delaware, the Certificate of Incorporation of the corporation shall be amended and restated in its entirety to read as set forth on Exhibit A attached hereto.

IN WITNESS WHEREOF, said corporation has caused this Certificate to be executed by a duly authorized officer this 23rd day of May, 2001.

By: _____
Gregory Williams
Chief Executive Officer

740322.2.01 5/24/2001 3:35 PM

STATE OF DELAWARE
SECRETARY OF STATE
DIVISION OF CORPORATIONS
FILED 04:15 PM 05/25/2001
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EXHIBIT A

# AMENDED AND RESTATED CERTIFICATE OF INCORPORATION

# OF

# INTERSIL COMMUNICATIONS, INC.

1. *Name.* The name of the Corporation is Intersil Communications, Inc.

2. *Registered Office and Agent.* The address of the Corporation's registered office in the State of Delaware is 1209 Orange Street, in the City of Wilmington, County of New Castle. The name of the Corporation's registered agent at such address is The Corporation Trust Company.

3. *Purpose.* The purposes for which the Corporation is formed are to engage in any lawful act or activity, including, without limitation, forming and/or acquiring foreign subsidiaries, for which corporations may be organized under the General Corporation Law of the State of Delaware ("DGCL") and to possess and exercise all of the powers and privileges granted by such law and any other law of Delaware.

4. *Authorized Capital.* The aggregate number of shares of stock which the Corporation shall have authority to issue is One Thousand (1,000) shares, all of which are of one class and are designated as Common Stock, par value $.01 per share.

5. *Incorporator.* The name and mailing address of the incorporator are Marian T. Ryan, 4000 Bell Atlantic Tower, 1717 Arch Street, Philadelphia, Pennsylvania 19103-2793.

6. *Bylaws.* In furtherance and not in limitation of the powers conferred by law, the board of directors of the Corporation is authorized to adopt, amend or repeal the bylaws of the Corporation, except as otherwise specifically provided therein, subject to the powers of the stockholders of the Corporation to amend or repeal any bylaws adopted by the board of directors.

7. *Elections of Directors.* Elections of directors need not be by written ballot unless and except to the extent the bylaws of the Corporation shall so provide.

8. *Right to Amend.* The corporation reserves the right to amend or repeal any provision contained in this Certificate as the same may from time to time be in effect in the manner now or hereafter prescribed by law, and all rights, preferences and privileges conferred on stockholders, director or others hereunder are subject to such reservation.

9. *Unanimous Written Consent Required.* If any action is to be taken by stockholders without a meeting, such action must be authorized by unanimous written consent signed by all of the holders of outstanding voting stock.

10. *Limitation on Liability.* The directors of the Corporation shall be entitled to the benefits of all limitations on the liability of directors generally that are now or hereafter become available under the DGCL. Without limiting the generality of the foregoing, to the fullest extent permitted by the DGCL, as it exists on the date hereof or as it may hereafter be amended, no director of the Corporation shall be personally liable to the Corporation or its stockholders for monetary damages for breach of fiduciary duty as a director, except for liability (i) for any breach of the director's duty of loyalty to the Corporation or its stockholders, (ii) for acts or omissions not in good faith or which involve intentional misconduct or a knowing violation of law, (iii) under Section 174 of the DGCL, or (iv) for any transaction from which the director derived an improper personal benefit. Any repeal or modification of this Section 10 shall be prospective only, and shall not affect, to the detriment of any director, any limitation on the personal liability of a director of the Corporation existing at the time of such repeal, modification or adoption.

Dated: May 23, 2001

By: _____
Gregory L. Williams
Chief Executive Officer

# PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

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|---|---|
| SUBMISSION TYPE: | NEW ASSIGNMENT |
| NATURE OF CONVEYANCE: | ASSIGNMENT |

CONVEYING PARTY DATA

| Name | Execution Date |
|---|---|
| INTERSIL COMMUNICATIONS, INC. | 12/21/2001 |

RECEIVING PARTY DATA

| | |
|---|---|
| Name: | INTERSIL AMERICAS, INC. |
| Street Address: | 1001 MURPHY RANCH ROAD |
| City: | MILPITAS |
| State/Country: | CALIFORNIA |
| Postal Code: | 95035 |

PROPERTY NUMBERS Total: 2

| Property Type | Number |
|---|---|
| Patent Number: | 4823173 |
| Patent Number: | 5264719 |

CH $80.00 4823173

CORRESPONDENCE DATA

Fax Number: (703)931-6037
*Correspondence will be sent via US Mail when the fax attempt is unsuccessful.*
Phone: 2022363707
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Correspondent Name: Wallace G. Walter
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Address Line 4: Alexandria, VIRGINIA 22311

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| NAME OF SUBMITTER: | Wallace G. Walter |

Total Attachments: 4
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source=IntersilContribAgmt#page3.tif
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# CONTRIBUTION AGREEMENT

This Contribution Agreement (the "Agreement") is effective as of December 31, 2001 (the "Effective Date") at 11:59 PM United States of America EST (the "Effective Time") by and between Intersil Communications, Inc., a Delaware corporation ("Intersil"), and Intersil Americas Inc., a Delaware corporation ("Intersil Americas").

## Background

To promote greater efficiency and economy in the management of the businesses carried on by the parties to this Agreement, Intersil desires to make a capital contribution to Intersil Americas of certain intellectual property and other assets used in the business of Intersil and its affiliates.

## Terms

Intending to be legally bound, the parties to this Agreement agree as follows:

1. Effective as of the date first written above, Intersil shall contribute the following to Intersil Americas, in deemed exchange for stock of Intersil Americas in a non-recognition transaction as described in Section 351 of the Internal Revenue Code of 1986, as amended:

(i) all right, title and interest in and to the trademarks shown in Schedule A and all slogans, logotypes, designs, and trade dress associated therewith (the "Trademarks"), together with the U.S. federal registrations and applications for registration of the Trademarks, in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto and in and to all rights of action arising from the Trademarks, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made, and the goodwill of the business symbolized by the Trademarks;

(ii) all right, title and interest in and to the U.S. patents and patent applications shown in Schedule A (the "Patents"), including all reissues, divisions, continuations, continuations-in-part, and extensions thereof, to be held and enjoyed by Intersil Americas as fully and entirely as they would have been held and enjoyed by Intersil if this contribution had not been made, including all licenses of and proceeds from the Patents, all claims, demands and rights to recovery that Intersil has or may have in profits and damages for past and future infringements, if any, and all rights to compromise, sue for, and collect such profits and damages;

(iii) all right, title, and interest in and to all inventions shown in Schedule A (the "Inventions"), and all intellectual property rights relating thereto, including, without limitation, trade secret rights in the Inventions, and all rights of action arising from the Inventions, to be held and enjoyed by Intersil Americas for its own use and benefit and for its successors and assigns as the same would have been held by Intersil had this contribution not been made; and

(iv) all right, title, and interest in and to all copyrights owned by Intersil as of the date first written above that are not otherwise excluded from contribution under the terms of this Agreement, whether or not such copyrights have been registered (collectively, the "Copyrights")

including, without limitation, all U.S. registrations and applications for registration of the Copyrights, all licenses of and proceeds from the Copyrights, all publishing, electronic publishing, and other proprietary rights arising from or related to the Copyrights, all causes of action relating to the Copyrights that may have arisen prior to this contribution, and any recovery resulting from such causes of action.

Notwithstanding the foregoing or any specific item listed on Schedule A, the intellectual property used in connection with providing products or services that are regulated by the United States Department of State shall not be contributed to Intersil Americas.

2. Intersil and Intersil Americas shall each take any and all additional actions as may be necessary or appropriate to effect the transactions contemplated by this Agreement. Such actions may include, without limitation, the execution of additional documents to record the contribution made in this Agreement and the filing of such documents with the appropriate governmental authorities.

[Signatures commence on the following page]

IN WITNESS WHEREOF, the parties have caused this Agreement to be executed as of the date below to be effective as of the Effective Date and Effective Time.

INTERSIL COMMUNICATIONS, INC.
a Delaware corporation

By: _____ Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

INTERSIL AMERICAS INC.
a Delaware Corporation

By: _____ Date: 12/21/01
Name: PAUL A. BERNKOPF
Title: ASST. SECRETARY

## SCHEDULE A
### (i) PATENTS AND PATENT APPLICATIONS

| ClientRef | SubCase | Status | Apl # | FilDate | Pat# | IssDate | Title |
|---|---|---|---|---|---|---|---|
| SE-358 | | Granted | 774474 | 10-Sep-1985 | 4677321 | 30-Jun-1987 | A TTL COMPATIBLE INPUT BUFFER |
| SE352 | | Granted | 793316 | 31-Oct-1985 | 4682059 | 21-Jul-1987 | A COMPARATOR INPUT STAGEFOR INTERFACE WITH SIGNAL CURRENT |
| SE-359 | | Granted | 782691 | 01-Oct-1985 | 4650696 | 17-Mar-1987 | PROCESS USING TUNGSTEN FOR MULTILEVEL METALIZATION |
| SE-363 | | Granted | 936609 | 01-Dec-1986 | 4781853 | 01-Nov-1988 | METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS |
| SE-363 | A | Granted | 187268 | 28-Apr-1988 | 4859280 | 22-Aug-1989 | METHOD OF ETCH & ENHANC SILICON ETCHING CAP OF ALKALI HYDROXIDE THROUGH ADD OF POSITIVE VALENCE IMPURITY IONS |
| SE-370 | | Granted | 723238 | 15-Apr-1985 | 4705596 | 10-Nov-1987 | SIMULTANEOUS PLASMA SCULPTURING AND DUAL TAPERED VIA ETCH |
| SE377 | | Granted | 782689 | 01-Oct-1985 | 4636744 | 13-Jan-1987 | FRONT END OF AN OPERATIONAL AMPLIFIER |
| SE704 | | Granted | 771712 | 03-Sep-1985 | 4624749 | 25-Nov-1986 | ELECTRODEPOSITION OF SUBMICROMETER METALLIC INTERCONNECT FOR INTEGRATED CIRCUITS |
| SE-705 | | Granted | 768326 | 22-Aug-1985 | 4716071 | 29-Dec-1987 | METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES |
| SE-705 | A | Granted | 045526 | 04-May-1987 | 4713260 | 15-Dec-1987 | METHOD FOR ENSURING ADHESION OF CHEMICALLY VAPOR DEPOSITED OXIDE TO GOLD INTEGRATED CIRCUIT INTERCONNECT LINES |
| SE-385 | | Granted | 896097 | 13-Aug-1986 | 4755770 | 05-Jul-1988 | LOW NOISE CURRENT SPECTRAL DENSITY INPUT BIAS CURRENT CANCEL SCHEME |
| SE-394 | | Granted | 723239 | 15-Apr-1985 | 4705597 | 10-Nov-1987 | PHOTORESIST TAPERING PROCESS |
| SE-395 | | Granted | 831384 | 07-Jan-1986 | 4823173 | 18-Apr-1989 | HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION |
| SE-395 | B | Granted | 07/705509 | 24-May-1991 | 5264719 | 23-Nov-1993 | HIGH VOLTAGE LATERAL MOS STRUCTURE WITH DEPLETED TOP GATE REGION |

**Patent License Agreement**

This Patent License Agreement ("PLA") is entered into on this 30th day of March, 2006 by and between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

1.

REDACTED

1.1

1.2

Power Integrations, Incorporated, including its parents, subsidiaries and consolidated entities (any or all of which, "POWI"). REDACTED United States Patent No. 4,823,173 and/or United States Patent No. 5,264,719, including any and all re-examinations, reissues or certificates of correction relating to such patents (collectively, the "Patents").

1.3

REDACTED

2.

2.1

REDACTED

2.2

3. **Additional Rights Granted Fairchild**

3.1 REDACTED Intersil grants to Fairchild the sole and exclusive right, exclusive even as to Intersil, to enforce the Patents against POWI, to assert, litigate and prosecute claims of Infringement under the Patents against POWI, including without limitation in any U.S. federal court or before the International Trade Commission, and to seek all equitable, injunctive, monetary and other relief and to collect for later distribution under Paragraph 1.2 any and all past damages in connection with Infringement of the Patents by POWI, and to settle and compromise any disputes with POWI related to the Patents. Except as provided herein, the Parties agree that only Fairchild shall have the authority to threaten, commence, maintain or settle any claim, suit or proceeding based upon Infringement of the Patents (or other trespass or similar action relating to the Patents and the inventions therein claimed) by POWI.

3.2

3.3

REDACTED

REDACTED

3.4

3.5

REDACTED

3.6

4. **Representations and Warranties**

4.1 Intersil represent and warrants as follows:

A. Intersil has the authority to enter into this PLA and to convey the rights conveyed herein, and that the execution and performance of this PLA does not conflict with Intersil's certificate of incorporation, by-laws or contract obligations.

B. Intersil is the sole owner of the Patents, the Patents have been and will be maintained, and that all inventors of the inventions claimed in the Patents have assigned title and ownership of the inventions to Intersil.

C.

4.2

A.

REDACTED

B.

C.

5. **Confidentiality**

The terms and conditions of this PLA, all communications, discussions and correspondence relating to this PLA, and all actions taken in performance of the PLA, shall be "Common Interest Information" covered by the Joint Defense and Confidentiality Agreement between the Parties, dated March 12, 2001, and shall be maintained in strict confidence in accordance with such Joint Defense and Confidentiality Agreement.

REDACTED

The parties have duly executed this Agreement as of the date first above written.

**INTERSIL CORPORATION**

By: _____

Name: _____

Title: _____

**FAIRCHILD SEMICONDUCTOR CORPORATION**

By: _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

The parties have duly executed this Agreement as of the date first above written.

**INTERSIL CORPORATION**

By: Douglas A. Balog

Name: DOUGLAS A. BALOG

Title: ASST. SECRETARY

**FAIRCHILD SEMICONDUCTOR CORPORATION**

By: _____

Name: Robert J. Conrad

Title: Senior Vice President – Analog Products

**Supplemental Agreement**

This Supplemental Agreement amends and, to the extent necessary, modifies *nunc pro tunc* the Patent License Agreement ("PLA") dated March 30, 2006 between Intersil Corporation ("Intersil") and Fairchild Semiconductor Corporation ("Fairchild") (collectively, the "Parties").

Intersil Americas, Inc. ("Intersil Americas"), as title holder of record of United States Patent No. 4,823,173 and United States Patent No. 5,264,719 (the "Patents"), hereby fully ratifies the terms of the March 30, 2006 PLA. Intersil Americas further acknowledges that its parent corporation, Intersil Corporation, was authorized to enter into the PLA on behalf of Intersil Americas, and to agree to the terms stated therein. Intersil Americas agrees to be bound by, and hereby reaffirms, the representations and warranties made by Intersil Corporation in the PLA.

It is the intent of the parties hereto that this Supplemental Agreement shall be retroactive to March 30, 2006, and shall have the effect of assigning and conveying from Intersil Americas to Fairchild, as of March 30, 2006, the specific rights to the Patents as detailed in the PLA as if Intersil Americas – and not Intersil Corporation – was the original party to the PLA. This Supplemental Agreement does not modify the substantive rights of Fairchild under the PLA, and the substantive rights afforded to Intersil Corporation under the PLA remain unchanged, but will be deemed to reside in Intersil Americas. Intersil Corporation shall remain bound under the PLA itself. This Supplemental Agreement does not alter the ongoing obligations, if any, of any Intersil related entity under the Asset Purchase Agreement and the related Intellectual Property Assignment and License Agreement between Intersil Corporation and Fairchild dated January 20, 2001. Intersil Americas assumes no obligations other than as expressly set forth herein and in the body of the PLA.

Executed on May 18, 2006, but effective March 30, 2006.

**INTERSIL CORPORATION**

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

**INTERSIL AMERICAS, INC.**

By: Douglas A. Balog
Name: DOUGLAS A. BALOG
Title: ASST. SECRETARY

**FAIRCHILD SEMICONDUCTOR CORPORATION**

By:
Name:
Title: